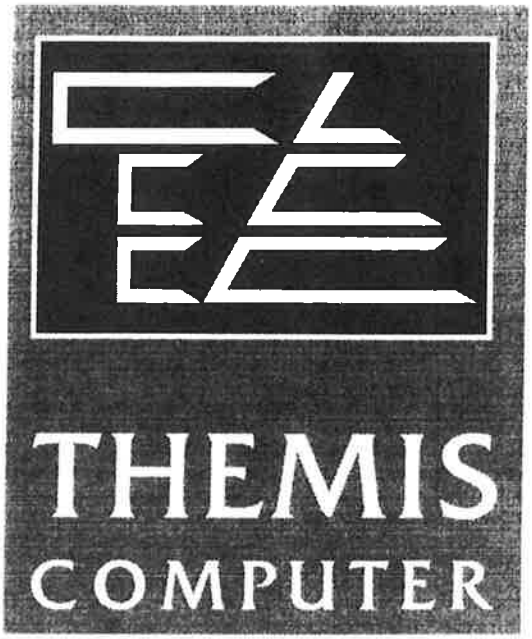


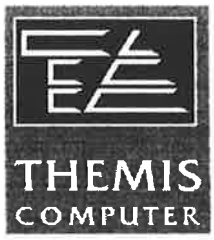
USP-I

Hardware Manual

Part Number: 106625

USP-I Hardware Manual

Version 1.0 (Rev. X1.3) —22 May, 1998



Themis Computer—Americas and Pacific Rim
3185 Laurelview Court
Fremont, CA 94538
Phone (510) 252-0870
Fax (510) 490-5529
World Wide Web http://www.themis.com

Themis Computer—Rest of World
1, Rue Des Essarts
Z.A. De Mayencin
38610 Gieres, France
Phone 33 76 59 60 61
Fax 33 76 63 00 30

Themis Customer Support

North America, South America, and Pacific Rim

Telephone: 510-252-0870
Fax: 510-490-5529
E-mail: support@themis.com
Web Site: http://www.themis.com

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1 Introduction

1.1 Introduction

Thank you for purchasing the Themis USP-1 single board computer with VMEbus interface. Themis Computer is a leading manufacturer of SPARC based processor boards for the VMEbus market. We value our customers comments and concerns. Our Marketing department is eager to know what you think of our products. A "Reader Comment Card" is located at the end of this manual for your use.

Caution — Before you begin, carefully read each of the procedures in this manual. Improper handling can cause serious damage to the equipment.

1.2 Scope

The purpose of this document is to provide a hardware overview of the USP-1. This manual is written for system integrators and programmers. It contains all the necessary information to install and configure the USP-1 processor board. It is assumed that the Sun Open Boot PROM (OBP) is installed. If you intend to use another operating system or a real-time kernel such as VxWorks, please consult the appropriate documentation accompanying your OS or kernel software.

The reader is assumed to be familiar with and have a working knowledge of the UltraSPARC-1 processor architecture, SPARCclassic chip-set, and current VMEbus, SBus, Ethernet, and SCSI specifications. Although all USP-1 specific hardware and software features are described in detail in this manual, programmers wishing to code the USP-1 without the benefit of an operating system or real-time kernel will require additional data sheets and documentation for the SPARCclassic chip-set and other system components comprising the USP-1 design.

1.3 USP-1 Systems Overview

The USP-1 is a high-end uni-processor desktop workstation based on Sun4u, formerly known as Sun5, system architecture.

Features of the USP-1 are

- 64-bit V9 UltraSPARC-1 processor, with system operating frequencies up to 100 MHz. The processor frequency is up to two (2) times the system frequency (200MHz).
- Use of Themis proprietary memory modules.
- UPA coherent memory interconnect.
- 2 serial ports supporting both synchronous and asynchronous protocols.
- 2 asynchronous mode serial ports for keyboard or mouse interface that can be configured as TTY C/D on the P2 connector.
- Centronic compatible parallel port interface.
- Built-in audio interface.
- 2 SBus expansion slots.
- 10 Mbyte/sec Ethernet.
- 10 Mbyte/sec SCSI.
- Supports the following memory modules: 128 Mbyte or 256 Mbyte memory modules.
- VME64 Interface

Related Documents - The reader should consult with the following documents if more detailed information is needed.

- Themis USP-1 Programmer's Guide
- SBus Reference Platform System Programmer's Guide
- American National Standard for VME64 ANSI/VITA1-1994
- Sun 4u System Architecture
- Standard for a Modular I/O Interconnect to support Futurebus+, VMEbus, and Desktop Computers -- IEEE1496
- UltraSPARC-I/II User's Manual
- U2S and UPA to SBus User's Manual
- Sun I/O chipset Reference Manual
- USC Uniprocessor System Controller User's Manual
- Tundra VMEbus Interface Components Manual, Spring 1996
- UPA Interconnect Architecture
- IEEE Std. 1149.1-1990, IEEE Standard Test Access Port and Boundary Scan Architecture
- IEEE Std 1149.16-1994, Supplement to IEEE Std. 1149.1-1990
- The SPARC Architecture Manual, Version 9.

1.4 Contents

This text is largely based on the Sun SBus Reference Document. Several chapters have been added to define the VMEBus.

Chapters 1 and 2 present an introduction to the USP-1.

- Chapter 1, "Introduction," presents a systems overview and description of the organization of the manual.
- Chapter 2, "Installation," provides instructions for the set-up and configuration of the USP-1. Described in this chapter are the installation of several peripheral items, configuration of the OpenBoot PROM (OBP), and warranty and registration information.

Chapter 3 - 5 present the details of the USP-1 that are specific to product.

- Chapter 3, "USP-1 Hardware Specifications," details the hardware specifications. It includes, but is not limited to environmental operating and storage specifications.
- Chapter 4, "Configuration and Options," describes the various jumper, solder bead, memory, and frequency options which are available to the customer from Themis.

Note — Themis distinguishes between two types of options: field options, which the customer may set in the field and factory options, which Themis sets before shipping the board or when the board is returned to Themis for re-configuration. Factory configurable options are not to be configured by the customer. An example of a field option is a jumper. An example of a factory option is a solder bead. Not all factory options are re-configurable and the customer should decide upon the desired configuration before shipment of the board.

- Chapter 5, "Connectors and Pinouts," present connector and pinout diagrams for the USP-1.

Chapter 6 - 12 presents information on the common components of the USP-1 and the SBus Reference System. These chapters are presented so the customer may obtain an background understanding of hardware in the USP-1. The customer will not have to configure these components.

- Chapter 6, "Hardware Overview," describes the major hardware components of the USP-1 including the UPA Interconnect, memory system, and I/O system.
- Chapter 7, "ASICs," is concerned with the Application Specific Integrated Circuits (ACIS) present on the USP-1. These include the UPA to SBus Interface (U2S), Cross Bar Switch (XB1), Reset, Interrupt, Scan, and Clock controller (RIC), Macio, Slavio, and the Aurora Personality Chip (APC).
- Chapter 8, "Reset," describes the sources and effects of hardware resets.
- Chapter 9, "Clocks" describes several clock present on the USP-1.
- Chapter 10, "Power Management" describes hardware and software power management systems.
- Chapter 11, "Initialization and Diagnostics" describes the initialization and diagnostic features of the USP-1. It also provides diagnostic test of the ethernet connect and further reference materials.
- Chapter 12, "JTAG" provides and overview of the JTAG system.

1.5 Getting Started

1.5.1 How to Start Quickly

This document presents the Theory of Operation of the USP-1. It is intended to be a general purpose guide to the USP-1 for system architects, programmers, technicians, and other users. Technical discussions begin from an architectural perspective of a given topic and then proceed to those aspects of a general Sun architecture as

it is implemented in the USP-1. board from a programmer's view. The information presented here is also written for the technician. In most cases, all that will be needed in the laboratory is this document and the appropriate toolkit. Finally the discussion retains a global view that is useful to a less technical user.

1.5.1.1 Product Warranty and Registration

Please review the computer warranty information packaged with your USP-1 processor board. Your USP-1 single board computer is automatically registered when it leaves the factory based on the information provided in the sales order. All computers are tracked via the serial number. The warranty service period is based on the original shipment date from the factory.

1.5.1.2 Unpacking the USP-1

Caution — The USP-1 contains statically sensitive components. Industry standard measures (use of a grounded wrist strap) must be observed when removing the USP-1 from it's shipping container and during any subsequent handling.

Remove the USP-1 and accessories from its shipping container and check the contents against the packing list. The package should include:

- Themis USP-1
- USP-1 Warranty Information
- Integration Kit (if ordered separately)
  - Paddleboard
  - A/B Serial Cable
  - Front Panel SCSI Cable
  - Flat Ribbon SCSI Cable
  - AUI Ethernet Cable
- USP-1 User Manual (if ordered separately).

Please report any discrepancies to the Themis Computer Customer Support department immediately.

1.5.2 In Case of Difficulties

Our Customer Support department is committed to providing the best product support in the industry. Customer support is available 8am - 5pm (PST), Monday through Friday via telephone, fax, e-mail or our World Wide Web site.

Themis Customer Support

Telephone: 510-252-0870
Fax: 510-490-5529
E-mail: support@themis.com
Web Site: http://www.themis.com

2

Installation

2.1 Registering

Please review the Themis Computer warranty and complete the product registration card delivered with your USP-1 board(s). Return of the registration card is not required to activate your product warranty but, by registering your USP-1, Themis Computer will be able to better provide you with timely updated information and product enhancement notifications.

At Themis Computer we value our customers comments and concerns. We have a marketing department that is eager to know what you think of our products and a customer support department that is committed to providing the best product support in the industry.

Customer support is available 8AM to 5PM PST, Monday through Friday via telephone, fax, email, or our web site.

Customer Support:

Phone: 510-252-0870 Fax: 510-490-5529

Email: support@themis.com

Web site: www.themis.com

2.2 Configuring the USP-1

Confirm the installation of all factory default jumpers. Refer to Chapter 4, Configurations and Options. The default configuration is as follows:

- USP-1 as Slot 1 System Controller
- Keyboard/Mouse ports connect to front panel
- Active SCSI termination enabled on base and I/O modules
- Drive / Receive SYSRESET*
- Serial Port A/B is EIA-232-E/EIA-423A compatible

- Boot from FLASH
- FLASH programming disabled
- Manual Ethernet port selection enabled
- Use normal twisted pair squelch threshold for 10BASE-T
- Bypass VMEbus interface in JTAG scan chain.

If the default jumper settings meet your requirements you are now ready to install the SPARC USP-1 in a standard VME chassis. To check the default configurations or if re-configuration is required, refer to Chapter 4, Configurations and Options, for information concerning board jumper settings, solder bead, and memory configurations.

Note — If you are not installing the USP-1 as a slot 1 system controller, jumper J1201 must be installed.

In addition to the USP-1 hardware a standard VME chassis with P1/P2 backplane is required. If you intend to use the USP-1 in a workstation configuration instead of as an embedded controller, you will also need a hard disk and graphics frame buffer or serial terminal.

2.3 OpenBOOT PROM Configuration

At power-up, the processor fetches instructions starting at one physical address 0x20 from the FLASH device.

In order to program the flash, the following OBP commands can be used:

```
update-flash <filename>
```

Note — Either the AUI or 10BASE-T port must be connected to a network with the proper server.

2.4 Configuring The VME Interface

Themis has implemented a variable and flexible VMEbus interface using both on-board jumpers, OpenBoot PROM (OBP) commands, and environment variables specific to the USP-1 board.

The USP-1 is typically re-configured when VMEbus boards are added, removed, or changed in the chassis. Board configuration normally involves allocation of VMEbus master access address, interrupts, and slave base address of the USP-1.

A small number of VME interface capabilities are configured using jumpers or solder beads, including:

- the slot-1 System Controller capability
- the VMEbus isolation

All other VMEbus interface related options are configured using extensions to the Sun OpenBoot PROM monitor program. OBP stores system configuration parameters in non-volatile storage (NVRAM) using a `setenv` mechanism familiar to UNIX shell users.

The default configuration upon delivery of the USP-1 (or after restoring the factory default values by pressing L1-N) is:

- VME slave accesses disabled
- VME slave base address at 0x00
- Mailbox interrupts disabled
- Mailbox interrupt at CPU level 9.

The OBP command `setenv` must be used to set the values of the environment variables. The `printenv` command will list all supported environment variables and can be used to verify proper setting. You must be at the OpenBoot command prompt to enter and execute OpenBoot commands.

If autoboot is enabled, interrupt the boot sequence by pressing L1-A (STOP-A); on an serial terminal press BREAK.

If BOOTMON compatibility mode is enabled, you will initially see the BOOTMON prompt. Enter `n` to start OpenBoot:

```
Type b (boot), c (continue), or n (new command mode)
>n
ok>
```

At the ok> prompt you are now able to enter OBP commands. Use `setenv` to modify the environment variables necessary to configure the USP-1 for your VMEbus configurations or execute the appropriate OBP commands listed above.

The following example moves the slave window for A32 accesses to 0x80000000 and enables slave accesses.

```
ok> setenv vme32-slave-base 0x8000.0000
```

The OBP automatically programs the SCV64 interface chip with the correct register values and retains your settings in NVRAM.

Warning — Unless you are familiar with the Forth Monitor and are experienced in interacting with your system PROM, restrict yourself to the most basic Forth Monitor operations. That is, to syncing your disks, ejecting floppies from the diskette drive, booting your system and configuring the VME interface. More advanced commands can do damage to your system's operation.

2.4.1 VMEbus Memory Allocation

The U2S SBus address space contains seven (7) physical SBus slots, with 256 MBytes assigned to each slot (Refer to USP-1 Programmer's Guide for the USP-1 Memory Map). Each slot is logically divided into sixteen (16), 16 MByte segments. Any unused 16 MByte segment may be mapped to the VMEbus address space through the VME MMU translation table located on the VSIC. Any segment allocated to the VMEbus can be programmed to access anywhere in the 4GByte VMEbus address space using any data path option supported by the SCV64 (i.e., A32:D32, A24:D32, A24:D16, A16:D16).

2.4.1.1 SBus Address Mapping

- **SBus Slot #0**

  This slot can be configured for SBus-only or programmable SBus / VMEbus on a per segment basis.

- **SBus Slot #1**

- This slot can be configured for SBus-only or programmable SBus / VMEbus on a per segment basis

- **SBus Slot #2**

  The entire 256 Mbyte address space is dedicated to the VMEbus. Each 16 Mbyte segment can be configured for a specific VMEbus target address and corresponding addressing mode and data width.

- **SBus Slot #3**

  MACIO #2

- **SBus slot #13**

  Audio (APC)

- **SBus slot #14**

  MACIO #1

- **SBus slot #15**

  SLAVIO

2.4.1.2 VME MMU Address Translation Table

The physical system I/O address space available to the USP-1 processor consists of seven SBus slots of 256 Mbyte each.

To facilitate flexible mapping of the SBus address space to selectable VMEbus address ranges, the seven SBus windows have been divided into a total of 112 segments of 16 Mbyte each, of which 100 segments may be mapped to the VMEbus.

Mapping of SBus to VMEbus accomplished by the VME MMU, a memory management unit maintained as a table of mapping specifiers.

The VME MMU table contains a 32-bit specifier entry for each 16 Mbyte segment, describing the segments mapping properties. Each specifier consists of:

- Target designation. SBus resources or VMEbus resources (unless selection is prohibited by hardware, as in the case of SBus Slots #0 and #1).
- Addressing mode (A32/A24/A16).
- Data width. Indicates D32 or D16 mode on VMEbus accesses.

- VME base address. The 16 Mbyte aligned base address generated on the VMEbus (for VME accesses only).

To facilitate easy configuration of the VME MMU table, a number of OBP commands have been added to allow interactive configuration of the VME MMU table. A configured VME MMU can then be permanently stored in NVRAM.

2.5 Installing The USP-1 Paddleboard

The paddle board delivered with the USP-1 attaches to the rear of the P2 backplane and provides industry standard connectors for Serial Ports C and D, Ethernet, SCSI, and printer.

The board contains no statically sensitive components but should be handled with care to avoid bending pins on the connectors.

Two P2 connectors allow secure installation of the paddle at the rear of the P2 backplane.

2.6 Attaching the USP-1 To A Network

The USP-1 features both a 10Base-T and AUI ethernet interface connectors. OBP determines the active interface upon power-up.

After attaching the USP-1 to a network, you can verify proper physical connection by executing the FORTH network selftest (test net). This test will indicate external loopback failure on each of the network interfaces when there is not a proper physical connection. As only one interface can be active, the inactive network interface will always return an external loopback error.

```
ok> test net

Using AUI Ethernet Interface
Lance Register test -- succeeded
Internal loopback test -- succeeded
External loopback test -- Lost Carrier (transceiver cable problem?)
send failed

Using TP Ethernet Interface
Lance Register test -- succeeded
Internal loopback test -- succeeded
External loopback test -- succeeded
send ok
net selftest succeeded
```

2.7 Attaching a Keyboard and Mouse

A standard SUN type 4 or type 5 keyboard/mouse combination can be attached to the front panel keyboard connector.

Note — The POST (power on self test) displays the message "`Warning: no keyboard detected`" if no keyboard is attached to the USP-1. This message may alternately indicate that configuration jumpers J5203 and J5204 are not configured for the front panel mouse/keyboard interface.

3

Hardware Overview

3.1 Overview

This chapter provides a brief hardware overview of the USP-1. Detailed information about each component can be found in the respective component specification. Operations of individual peripheral devices will not be covered.

The UPA interconnect provides interconnection at the highest level. Components interfacing through the UPA interconnect are processor subsystem, System Controller, Buffered Crossbar Chip, memory, and I/O subsystem. Processor sub-system includes the UltraSPARC-1 processor, E-cache Tag and Data RAM, and the UDBs. The System Controller provides overall control to the UPA interconnect and memory. The I/O sub-system consists of the SCV64, VMEbus, U2S, SBus slots, MACIO, SLAVIO, APC/CS4231, and other on-board devices. The RIC ASIC is independent of system interconnects. It provides JTAG, reset and clock control functions that are important to the system. The RIC ASIC communicates with other chips through direct interfaces.

3.2 Themis USP-1 Block Diagram

The CPU board at the block level is described below:

- Processor - a uni-processor system with the processor sub-system on the CPU board.
- SBus Slots - supports up to two external SBus slots.
- Memory Modules - supports one 128 MByte and up to four 256 MByte Memory Modules.

Figure 3-1 USP-1 Block Diagram on page 3-2 shows a block diagram of the USP-1 CPU board.

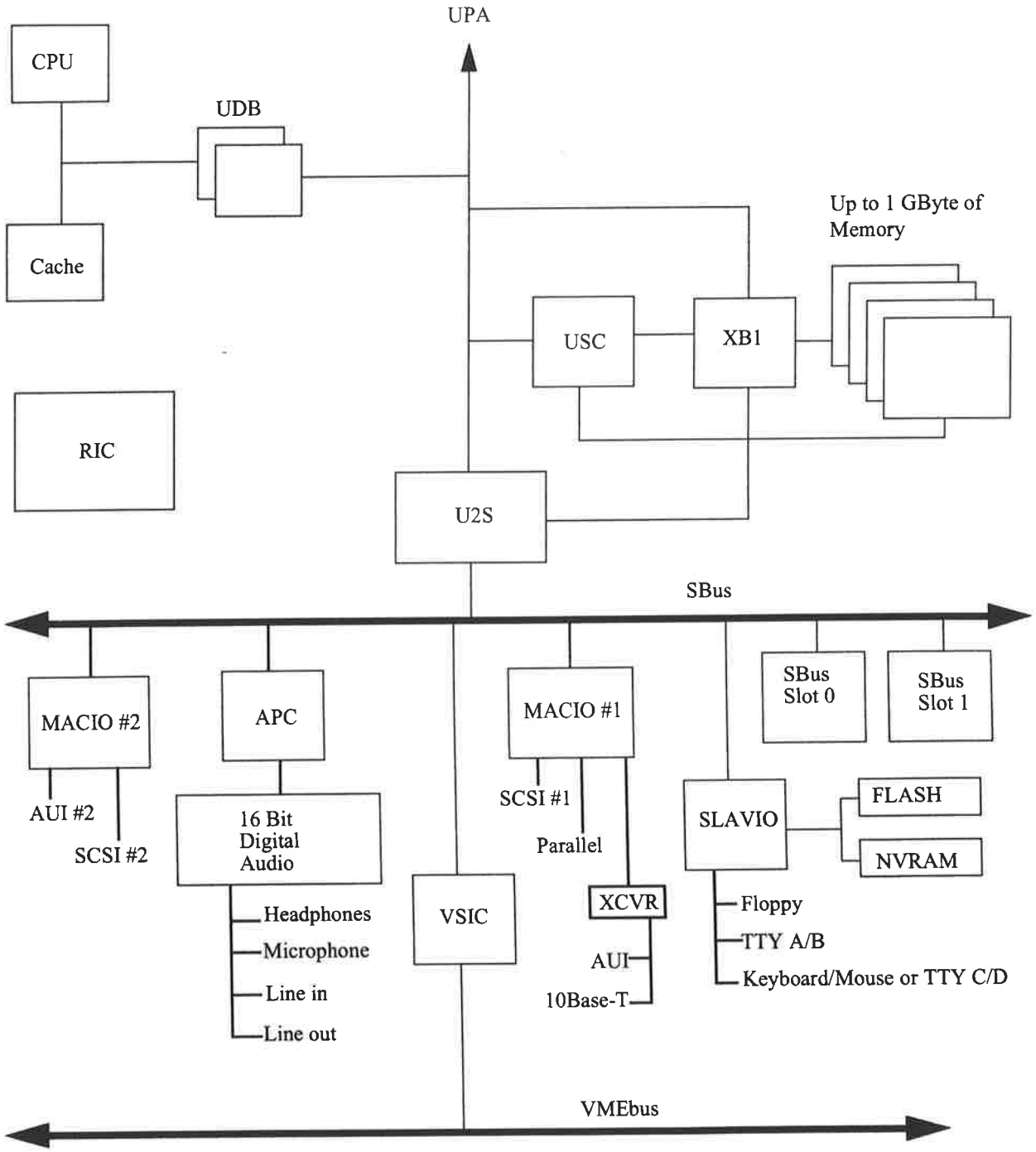


Figure 3-1. **USP-1 Block Diagram**

3.3 UPA Interconnect

Note — Throughout the UPA documentation, the term MID, master ID, is used. At times this is confusing because it is really a UPA *port* ID. For devices which are masters, there is no difference between port ID and master ID; however, devices which are slaves only have a port ID. Slave Devices can not have a Master ID. Port IDs are unique.

3.3.1 UPA Interconnect Overview

The UPA interconnect is a packet based, cache coherent interconnect. Non-coherent operations are also provided for accesses to I/O devices and other devices that do not support cache coherency. The physical connection among devices can be a bus or point to point. The USP-1 adopts multiple buses to achieve cost / performance requirements. The major components defined in the UPA Interconnects are UPA Ports, System Controller, Data Path and Memory. Physical connections among these devices are provided by Address Bus, Data Bus and Data Path Control, and Snoop Bus. A distributed arbitration algorithm is used to arbitrate among master ports sharing the same Address Bus. It is described in Chapter 3.3.5, UPA Arbitration.

Each UPA port can support one or more of the following functions: master, slave, interrupter, and interrupt receiver. A UPA master is a device capable of issuing UPA transactions to the interconnect. A UPA slave receives and services transactions requested by a UPA master or the System Controller. An interrupter is a device capable of generating interrupts to the interconnect and handling interrupt flow control as defined by the interconnect. An interrupt receiver is a device capable of handling interrupt and providing necessary flow control on interrupt packet across the interconnect.

The System Controller is the key element of the UPA interconnect. The services it provides are coherence control, memory control, datapath control, flow control, transaction ordering, and address routing. A brief description of the System Controller will be provided in a later section.

Figure 3-2 shows the physical connections among UPA devices in the USP-1 system. The following sections provide introductory information about the UPA. For more detailed description of how the UPA works, please refer to 'UPA Interconnect Architecture'.

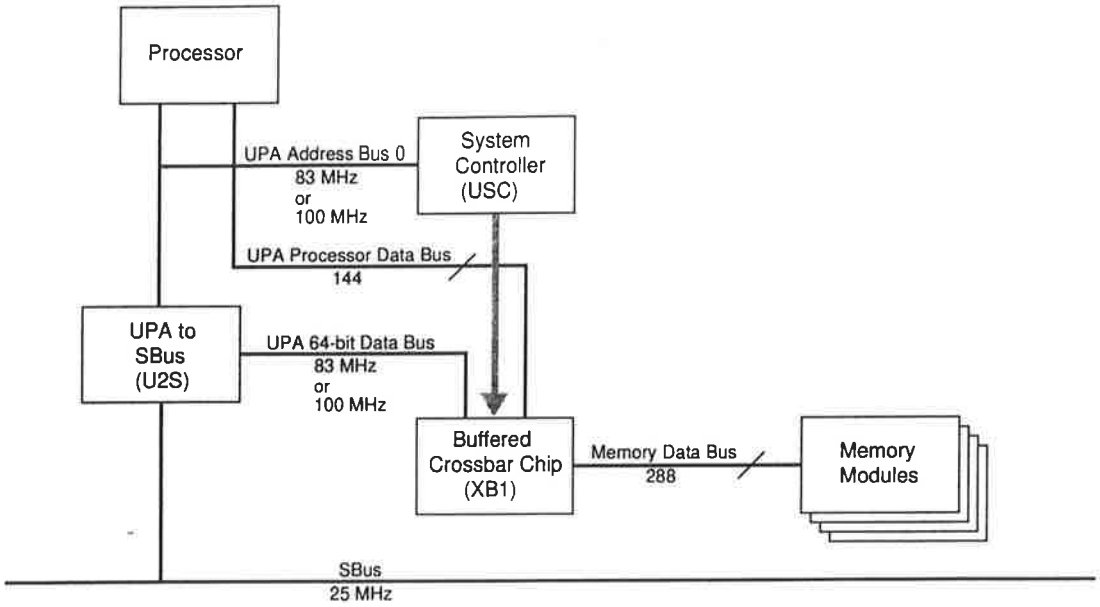


Figure 3-2. **UPA Interface Block Diagram**

3.3.2 UPA Data Transfer

Data transfers can happen between UPA devices or between a UPA device and memory. Data transfer is initiated by the master interface of a UPA port. The UPA port first asserts a request and waits for its turn to get the ownership of UPA Address Bus. It then sends a transaction request to the UPA Address Bus together with UPA_Addr_Valid signal. Examples of simplified data transfer operations are given here to help in understanding how the UPA works.

- **Non-cacheable Read:** The System Controller decodes the request packet and makes a transaction request to arbitrate for the address bus where the selected device resides. It then forwards the packet to the UPA slave. The UPA slave services the request and returns a P_Reply to the System Controller when data is available or there is an error. The UPA slave must respond to the transaction request which is directed to it. Failing to do so may cause the system to hang. Based on the P_Reply received, the System Controller schedules the datapath and sends a separate S_Reply to both parties involved in the transaction. The S_Reply tells the UPA slave to send data on the data bus and UPA master to receive data from the data bus.
- **Non-cacheable Write:** The System Controller forwards the request packet to the UPA slave. It then schedules the datapath and issues a separate S_Reply to both UPA master and UPA slave. The S_Reply tells the master port to drive data to its data bus and slave port to receive data from its data bus. Either the address packet or data can arrive to the slave port earlier than the other. If the slave port needs to use the data to schedule internal operations, it has to wait until data is received on its UPA port. After the slave port drains the data out of its UPA port interface, it can send a P_Reply to the System Controller. The purpose of this P_Reply is to provide flow control of data. It informs the System Controller that it has room for further incoming data. Precise transfer errors cannot be reported by a P_Reply. The error will be dropped, or reported as an interrupt.
- **Coherent Read:** When the System Controller detects a coherent request, it will perform a snoop operation to the external dual tag if DTAG is provided. It also starts a memory request in parallel with snoop operation. In the case of a snoop miss, data will be provided by memory. The System Controller

schedules the datapath based on the availability of memory data and issues S_Reply to the requesting master. In the case of a snoop hit, the System Controller issues a copyback, or copyback invalidate request to the UPA port that owns the block. If the coherent read also requires invalidation of another cache, invalidate requests will be issued to other UPA ports that also have this block in their cache. When the UPA slave port is ready to send out copyback data, it issues a P_Reply to the System Controller. If no invalidation is involved, the System Controller will schedule the datapath and issue a S_Reply to both the UPA slave port and the UPA master port to send / receive data. Otherwise, the System Controller has to wait until all invalidate operations are completed before issuing a S_Reply.

- **Coherent Write:** Coherent write requests are handled in the same fashion as coherent reads. The tag state is updated in the dual tags.

3.3.3 UPA Address Bus

The UPA Address Bus is a 35-bit wide packet-switched bus. The address bus is protected by a parity bit (UPA_Address_Parity). Odd parity is generated by the UPA masters; that is, the total number of bits, including parity, is odd. The UPA address bus carries transaction request packets generated by the master ports. The packet includes information such as transaction type, address, class, master ID (MID), and others.

Forty-one bits of physical address are carried in the packet, bits <40:4> come directly from the packet. Bits <3:0> can be derived from the 16 bits of Byte Mask field in the packet. The Master ID is a 5-bit field used to identify the master that initiated the transaction. Each slot gets its port ID from hardwired inputs to the UPA connector, from a software programmable register (in the case of U2S), or from its implicit location in the system. *Table 3-1* below shows the UPA Port ID assignments in the USP-1 system.

Table 3-1. **UPA Port ID Assignments**

UPA Slot Number	UPA Port ID <4:0>
Processor slot 0	0x0
U2S	0x1F

The UPA interconnect allows multiple UPA address busses in the system. UPA address bus 0 is shared by the processor port(s) and U2S. The System Controller is the only master device on the bus. Arbitration among device in accessing the address bus 0 is described in a later section. The USP-1 does not implement a second address bus used for graphics.

The UPA interconnect uses geographical addressing to select the target device. Each port is assigned with an address range to respond to. The System Controller hardwires the address range of each UPA slave port and routes UPA packets to the proper destination. The UPA_Address_Valid signal is driven active to indicate a valid address on the address bus.

Associated with each address packet is a reply packet. There are two sets of reply signals for each UPA port: a UPA port reply and a System Controller reply. Each port has to supply dedicated UPA port reply signals to the System Controller. The System Controller also needs to supply each port with a dedicated System Controller reply signals. UPA protocol requires that each UPA device respond to the access targeted to its slave port. Failure to reply to a slave access may hang the system indefinitely. The encoding of replies is such that connected ports indicate a PREPLY code representing idle immediately after reset. Unconnected ports normally return a PREPLY code of "UPA read time out," if they are present. Ports which are present must return idle after being reset. Any other code is interpreted as device not present.

3.3.4 UPA Data Bus

The UPA data bus provides data path connections between both UPA ports and memory and among UPA ports themselves. Three data busses, the processor data bus, the memory data bus, and the UPA 64-bit data bus, are implemented in USP-1 systems. They are interconnected by the Buffer Crossbar chip (XB1).

The Processor data bus is 144 bits wide with 128 bits of data and 16 bits of ECC check bits. The Memory data bus, connecting the memory modules and the XB1 chip, is 288 bits wide with 256 bits of data and 32 bits of ECC check bits. The UPA 64-bit data bus provides connection between the U2S and the XB1 chip. It is 72 bits wide with 64 bits of data and 8 bits of ECC check bits.

3.3.5 UPA Arbitration

The UPA Interconnect uses a distributed arbitration protocol to decide which master port has the ownership of the UPA address bus. It allows a maximum of four UPA master ports and an System Controller port. Every master interface has its own arbitration logic and uses the same algorithm. The master interfaces run synchronously. -

Each master port presents one request and that request is connected to all other master ports and the System Controller. The System Controller also provides a request that is connected to all the UPA master ports. System Controller requests have a higher priority than other ports in order to access the address bus if multiple requests are active at the same time. Among other master ports, the priority assignment is based on round-robin according to the value of current master. No matter which master port gets ownership of the bus, the value of current master is incremented by 1 and wraps around to 0 after it reaches 3. The current master has to give up the bus when another request is asserted.

3.3.6 Processor Sub-system

The USP-1 is a next-generation SPARC CPU incorporating, on chip, 16 KByte Instruction and 16 Kilobyte Data caches, integrated Level 2 cache management, a floating point unit, fixed point units, multi-instruction issue logic, and a 128-bit wide data bus.

The processor requires external synchronous SRAMs for the second level cache plus cache tags, and two data bus interface chips (UDBs). The processor complex is soldered onto the motherboard.

3.4 Memory System

The USP-1 memory system consists of three major components:

- the System Controller
- DRAM Memory Modules
- Buffered Crossbar Chips (XB1).

Figure 3-3 shows the USP-1 memory system block diagram.

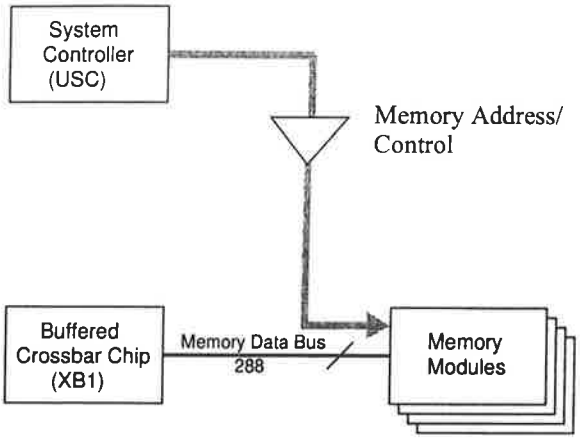


Figure 3-3. **Memory System Block Diagram**

3.4.1 System Controller

The System Controller contains several major blocks:

- Port Interface Controller (PIF)
- Data Path Scheduler (DPS)
- Memory Controller (MC)
- EBus.

3.4.1.1 Port Interface Controller (PIF)

This block of logic considers all UPA transactions and determines the intended target of the transaction. The PIF is responsible for the control flow for packets. It also performs the function of the Coherence Controller (CC).

3.4.1.2 Data Path Scheduler (DPS)

The Data Path Scheduler (DPS) controls all of the data flow in the machine coordinating the activity of the XB1 chips.

3.4.1.3 Memory Controller (MC)

This block implements all of the memory control for the system. All operations affecting DRAM are contained in this block. These include sizing, timing, and refresh

3.4.1.4 EBus

Since pins are limited on the USC a low pin count interface was chosen. This block provides an interface to the generic bus. Reset functionality is located in this block.

3.4.2 Buffered Crossbar Chip (XB1)

The Buffered Crossbar Chip (XB1) is the hub of all data transfers in the system. It coordinates activity among memory (at 288 bits wide), the processor UPA bus (at 144 bits wide), and the system UPA bus (at 72 bits wide). Transfers can take place among any of the ports. To minimize the cost, the chip is bit-sliced such that 18 parts are required to implement a full connection to the system.

3.5 I/O System

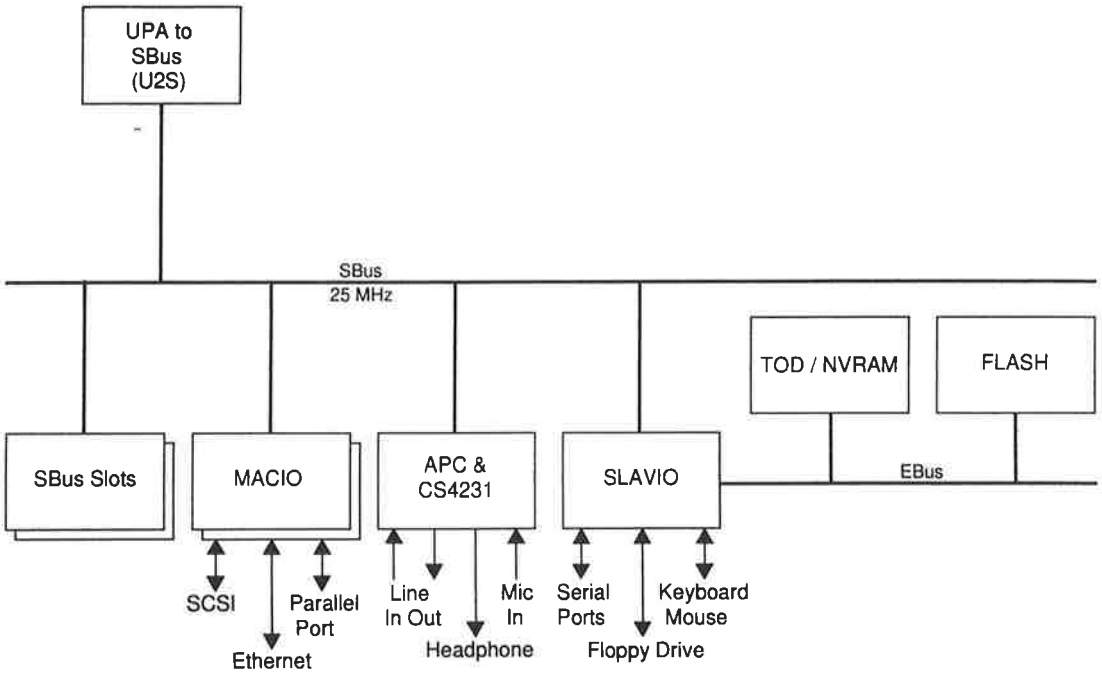


Figure 3-4. **I/O System Block Diagram**

3.5.1 U2S

The U2S is the bridge chip between the UPA and the SBus. In addition to providing simple bridge functions, it acts as the I/O hub and provides such necessary features as the IOMMU and Streaming Buffers. This is done to speed up sequential I/O accesses.

3.5.1.1 PIO Operation

A processor which wishes to access the SBus makes a UPA request which is forwarded to the U2S. The U2S processes the request, and if it is intended for the SBus, routes it down to that bus. Write operations are buffered. Errors are reported asynchronously. Refer to Chapter 9 of the Programmer's Guide, Error Handling, for more details on the error behavior.

Note — Hardware detection of synchronization between DVMA writes and PIO reads to the SBus is not provided.

3.5.1.2 DVMA Operation

All DMA transactions from SBus are actually DVMA transactions. This means that a virtual address is put on the SBus, and the U2S chip performs translation of that virtual address into a physical address recognized by the system. Translation is performed by the IOMMU. Bypass is provided for when translation is not desired.

3.5.1.3 Interrupt Dispatching

All interrupts on the UPA are performed as transactions (packets). The U2S works in conjunction with the RIC ASIC to translate level sensitive interrupts into packets which are delivered to the processor. Registers are present to control the mapping between the physical interrupt wire, and the corresponding code delivered in the interrupt packet. Registers also control the target of the interrupt. Interrupt transactions which go out on the UPA will never pass DVMA transactions which occurred prior to the interrupt. DVMA transactions may pass an interrupt.

3.5.1.4 UPA Interface

The U2S implements a 72 bit UPA interface.

3.5.1.5 ECC Checking / Generation

All packets to or from the UPA have ECC. The U2S logic performs ECC generation and checking.

3.5.1.6 SBus Interface

One of the major functions of the U2S is to bridge the UPA and SBus. It implements an IEEE P1496 compliant SBus interface.

3.5.1.7 Streaming Buffer

Streaming Buffers perform read-ahead / write-behind transfers to speed up sequential I/O activity. The transfers act to buffer data on the way to or from memory.

3.5.1.8 IOMMU

As mentioned in *§ 3.5.1.2 DVMA Operation*, the IOMMU performs translation between the virtual SBus address and a physical address. In addition, it supports bypass operation for devices not needing address translation, and pass through when not enabled.

3.5.1.9 Timer / Counter

Two Timer / Counters generate interrupts when the counter matches the programmed timer value and are useful for interrupting the system at specified intervals in the future. Two Timer / Counters are provided by the U2S.

3.5.2 MACIO #1 and #2

The MACIO chips implement the SBus interface to three master I/O devices: Ethernet, SCSI, and the parallel port. It contains three DMA channels implemented in its DMA2 block, one for each device supported.

Note — On MACIO #2, the parallel port is not supported.

3.5.3 Audio (APC)

The APC audio chip supports 16-bit digital audio along with an SBus interface. It provides an interface to a 16 bit CODEC with DMA.

3.5.4 SLAVIO

The SLAVIO is an I/O chip implementing three slave devices on the SBus. These are the serial ports, a keyboard / mouse, and the floppy disk controller.

3.5.5 EBus Devices

Auxiliary devices not conveniently fitting into an existing chip are implemented on the 8-bit expansion bus called the 'EBus'. Devices found on this interface include the Flash EPROM, the NVRAM/TOD chip, the System Controller interface, and the frequency margining registers.

3.6 RIC ASIC

The RIC ASIC contains logic for dock generation, reset control, interrupt concentration, and JTAG control.

3.7 USP-1 Flow Diagram

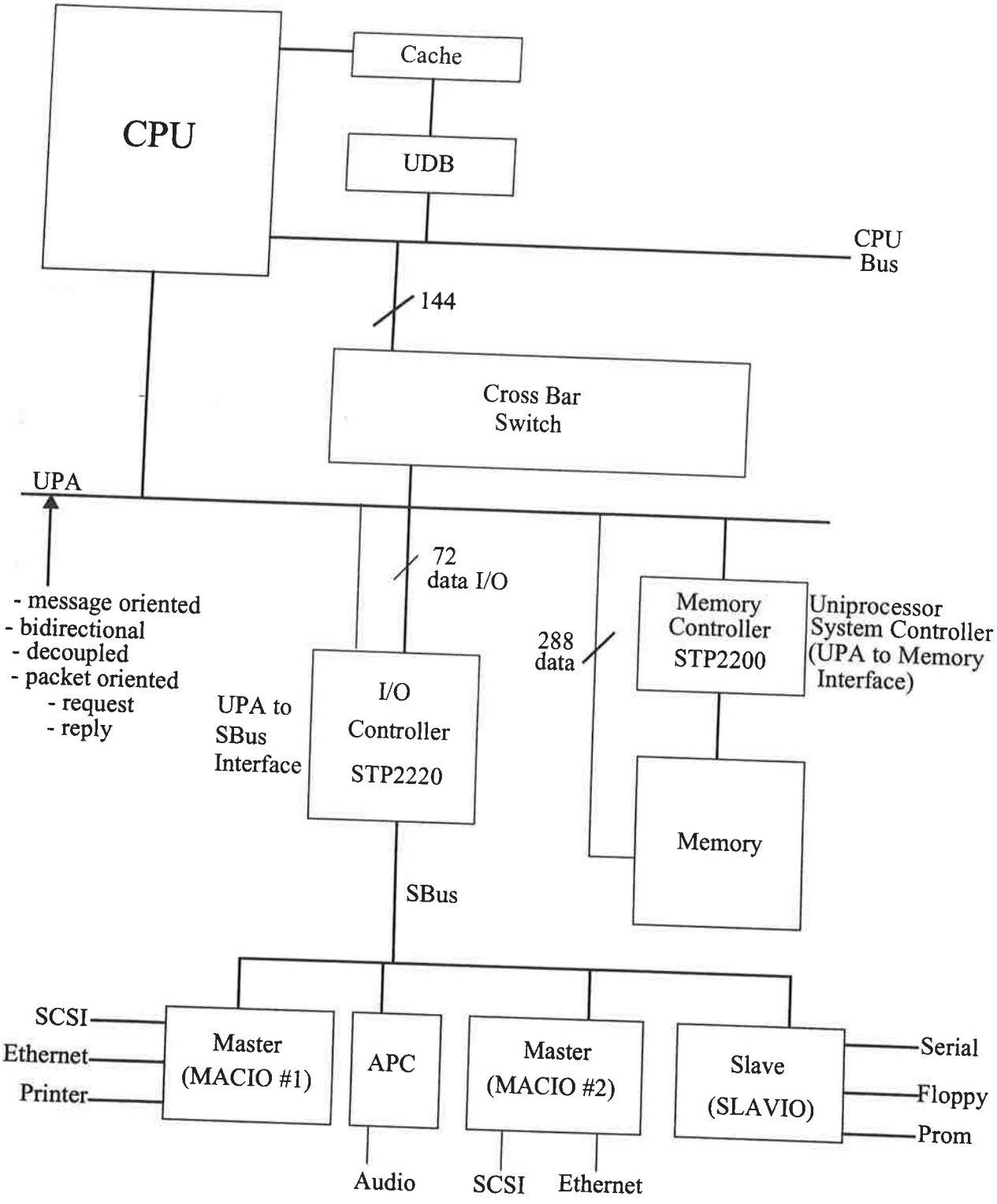


Figure 3-5. **USP-1 Flow Diagram**

3.8 User LEDs

The following table contains a description of the LEDs located on the front panel of the USP-1.

Table 3-2. **LED Description**

LED	Description
SCON	USP-1 is configured as a System Controller.
RUN	USP-1 is on
SD	USP-1 Over-temperature Shutdown
FAIL	SYSFAIL* asserted

4

Configurations and Options

This chapter is divided into 3 sections. The first, Configurations, describes the available configurations for the USP-1. These are memory configurations and must be set by Themis Computer.

The second section, Factory Options, reviews the various configuration options which must be set by Themis Computer. These options may not be altered by the customer. In order to change a factory configured item the USP-1 must be returned to Themis Computer for re-configuration.

The third section, Field Options, describes the various field configured items on the USP-1. These are primarily jumpers and switches. They may be set by the customer. There is no need to return the USP-1 to Themis for re-configuration of these items.

Note — If you have questions about the re-configuration of the USP-1, please contact Technical Support for more information.

4.1 Factory Configurables

4.1.1 Resistors Configurations

Table 4-1. **Resistor Configurations for setting UPA Clock Frequency**

Resistors	UPA Clock Frequency
R0113	UPA Clock frequency is 1/3 of CPU clock frequency
R0114 **(Default)**	UPA Clock frequency is 1/2 of CPU clock frequency
R2321	UPA Clock frequency is 1/3 of CPU clock frequency
R2322 **(Default)**	UPA Clock frequency is 1/2 of CPU clock frequency

Table 4-2. **Resistor Configurations for setting Cache Size**

Resistors	Cache Size
R0116 and R0115 **(Default)**	512 KBytes
R0109 and R0115	1 MByte
R0108 and R0109	2 MBytes

Table 4-3. **Resistor Configurations for CPU Clock Frequency**

Resistors	CPU Clock Frequency
R1422: R1424: R1426	133.33 MHz
R1422: R1424: R1425	143.00 MHz
R1422: R1423: R1426	153.90 MHz
R1422: R1423: R1425	166.66 MHz
R1421: R1424: R1426	181.88 MHz
R1421: R1424: R1425	200.00 MHz
R1421: R1423: R1426	222.00 MHz
R1421: R1423: R1425	250.00 MHz

Table 4-4. **Resistor Configurations for Frequency Generator**

Resistor	Description
R2344	Installed if SY89429 is installed at U2303
R2343	Installed if MC12429 is installed at U2303

Table 4-5. **Miscellaneous Resistor Descriptions**

Resistor	Name	Description
R1301 **(Default is Installed)**	Temperature Sensor Shutdown	When installed an over-temperature forces a CPU shutdown.

4.1.2 Solder Bead Configurations

4.1.2.1 I/O Board Solder Bead Description

Table 4-6. **I/O Board Solder Beads**

Solder Bead ID	Description
B5703	2-3, SCV64 directly drives SYSCLK
	1-2, reserved for the ASIC version of the VSIC
B5702	2-3, SCV64 directly drives BCLR*
	1-2, reserved for the ASIC version of the VSIC
B5701	2-3, SCV64 directly drives DTACK*
	1-2, reserved for the ASIC version of the VSIC
B5916	2-3, SCV64 directly drive RETRY*
	1-2, reserved for the ASIC version of the VSIC
B5915	2-3, SCV64 directly drives BBSY*
	1-2, reserved for the ASIC version of the VSIC
B5914	2-3, SCV64 directly drives SYSFAIL*
	1-2, reserved for the ASIC version of the VSIC
B5913	2-3, SCV64 directly drives BERR*
	1-2, reserved for the ASIC version of the VSIC
B5912	2-3, SCV64 directly drives SYSRESET*
	1-2, reserved for the ASIC version of the VSIC
B5911	2-3, SCV64 directly drives BR0*
	1-2, reserved for the ASIC version of the VSIC
B5910	2-3, SCV64 directly drives BR1*
	1-2, reserved for the ASIC version of the VSIC
B5909	2-3, SCV64 directly drives BR2*
	1-2, reserved for the ASIC version of the VSIC
B5908	2-3, SCV64 directly drives BR3*
	1-2, reserved for the ASIC version of the VSIC
B5907	2-3, SCV64 directly drives IRQ7*
	1-2, reserved for the ASIC version of the VSIC
B5906	2-3, SCV64 directly drives IRQ6*
	1-2, reserved for the ASIC version of the VSIC
B5905	2-3, SCV64 directly drives IRQ5*
	1-2, reserved for the ASIC version of the VSIC
B5904	2-3, SCV64 directly drives IRQ4*
	1-2, reserved for the ASIC version of the VSIC

Table 4-6. **I/O Board Solder Beads**

Solder Bead ID	Description
B5903	2-3, SCV64 directly drives IRQ3*
	1-2 Direct connection to VME ASIC
B5902	2-3, SCV64 directly drives IRQ2*
	1-2, reserved for the ASIC version of the VSIC
B5901	2-3, SCV64 directly drives IRQ1*
	1-2, reserved for the ASIC version of the VSIC

4.1.2.2 VSIC Board Solder Bead Description

The solder beads on the VSIC board are labelled with a "JP" designator.

Table 4-7. **VSIC Board Solder Beads**

Solder Bead ID	Description
JP1301	VSIC ID 0 (VID0)**
JP1302	VSIC ID 1 (VID1) **
JP1303	VSIC ID 2 (VID2) **
JP1304	VSIC ID 3 (VID3) **
JP1305	VSIC ID 4 (VID4) **
JP1306	VSIC ID 5 (VID5) **
JP1307	VSIC ID 6 (VID6) **
JP1308	VSIC ID 7 (VID7) **

Solder beads JP1301 - JP1308 are used to establish the VSIC ID number for different versions.

4.1.3 Solder Bead Locations

Note — Solder Bead locations are provided so the user may verify settings through visual inspection. Do not attempt to configure solder bead settings. If a solder bead setting needs to be altered, please contact technical support at Themis Computer. It will be necessary to temporarily return the board to Themis for re-configuration.

The '1' position on the solder bead is marked with a dark square.

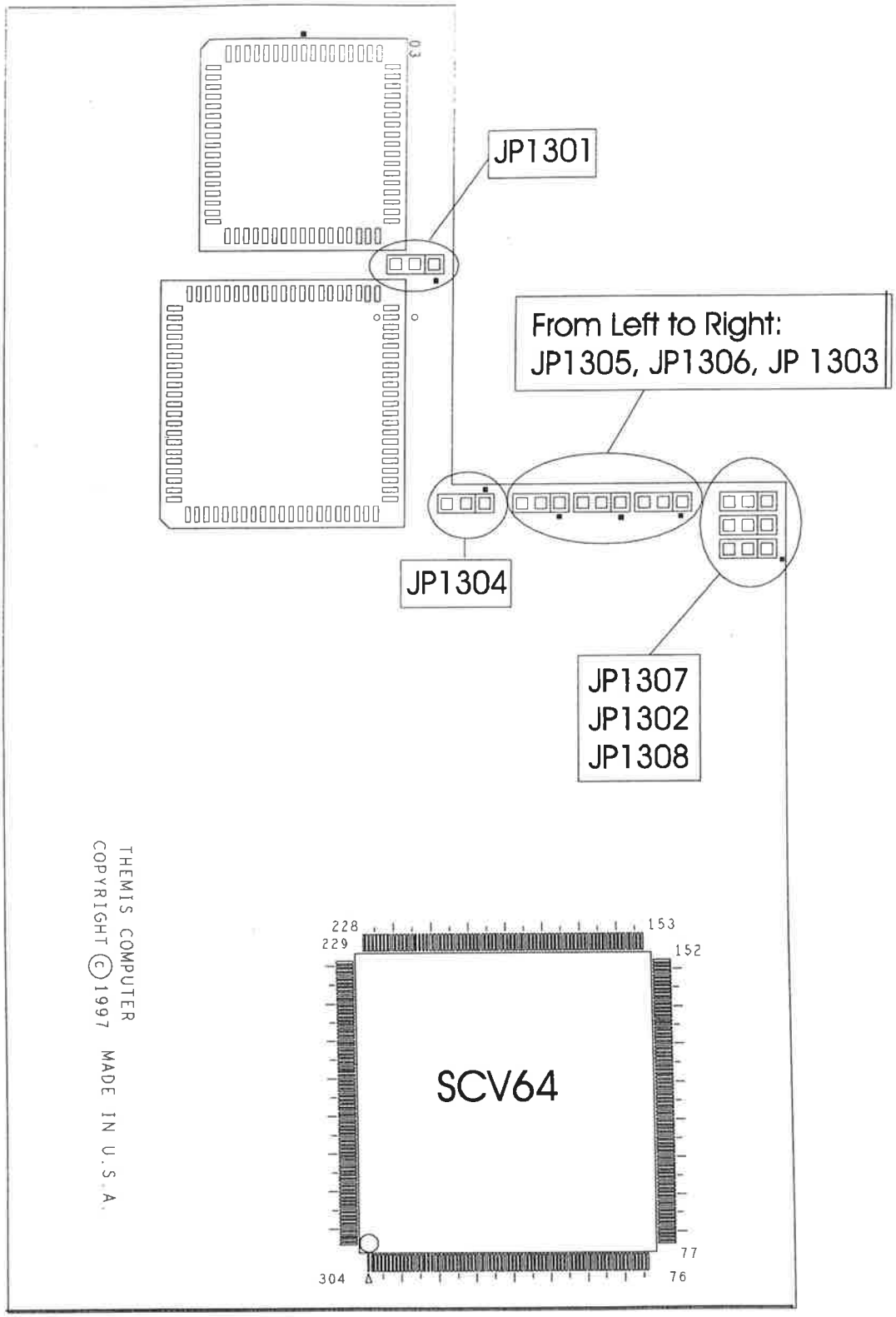


Figure 4-1. **Component Side: VSIC Board Solder Bead Location**

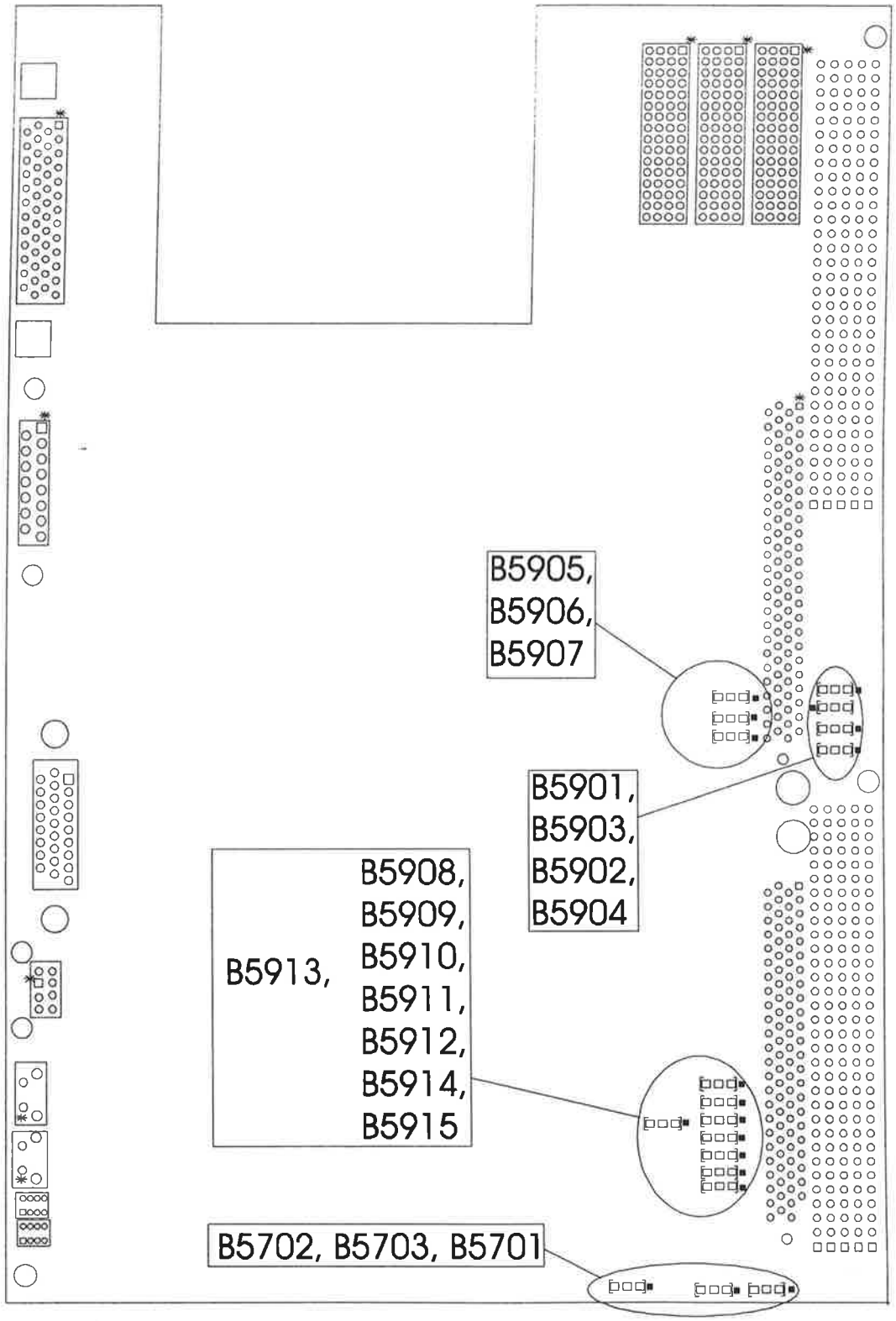


Figure 4-2. **Solder Side: I/O Board Solder Bead Locations**

4.2 Field Options

4.2.1 Memory Configurations

The USP-1 supports memory options of 128 MBytes, 256 MByte, 512 MByte, and 1 GByte.

The 256 MByte card has a configuration resistor to identify it as a top mounted or bottom mounted board.

Table 4-8. **256 MByte Memory Board Configuration Resistor**

Resistor ID	Description
R0722	Installed if the memory board is top mounted.
R0723	Installed if the memory board is bottom mounted.

4.2.2 Jumper Configurations

Jumper settings given in this chapter refer to etchings on the main logic board.

Jumpers are marked on the main logic board with part numbers. For example, the serial port jumpers are marked J2104 and J2105. Jumper pins are located immediately adjacent to the part number.

The following table contains a list of the jumpers used in the USP-1.

4.2.2.1 CPU Board

Table 4-9. **CPU Jumper Descriptions**

Jumper ID	Description
J4701	2-1 to disable Auxiliary SCSI termination.
	2-3 as a place holder **(Default)**

4.2.2.2 VSIC Board

Table 4-10. **Jumper List**

Jumper Number	Description
JP0401	Installed to enable Transmit / Receive of SYSRESET* to VMEbus **(Defualt)**
	Not Installed to disable Transmit / Receive of SYSRESET* VMEbus
J1201	Installed configures the USP-1 to be a Systems Controller **(Default)**
	Not installed configures the USP-1 not to be a System Controller

Table 4-11. **Slave Window Address Size**

JP1001	JP1002	Slave Address Window Size
Installed	Installed	128 MBytes
Installed	Not Installed	64 MBytes
Not Installed	Installed	32 M Bytes
Not Installed	Not Installed	8 MBytes

4.2.2.3 I/O Board

Table 4-12. **I/O Board Jumper Configurations**

Jumper ID	Description
J1101	1-2 to reduce Twisted Pair Ethernet signal output by 4.5 dB
	2-3 for normal Twisted Pair Ethernet audio output (Default) Same as uninstalled
J1102	1-2 for Automatic Selection between Twisted Pair and AUI Port **(Default)**
	2-3 for manual selection between Twisted Pair and AUI Ports through the MACIO[a]
JP2204	1-2 to swap upper and lower 256 KBytes of FLASH (Boot from the Lower Half of FLASH
	2-3 for normal partition of the FLASH **(Default)**
J5001	1-2: LED <3> LAMPTEST
	3-4: LED <2> LAMPTEST
	5-6: LED <1> LAMPTEST
	7-8: LED <0> LAMPTEST (Do not tie to Ground or else damage may result.)
JP5203	1-2 enables the port for Keyboard **(Default)**
	2-3 enables the port for TTYC
JP5204	1-2 enables the port for Mouse **(Default)**
	2-3 enables the port for TTYD
JP5202	1-2 to Enable SCSI terminator **(Default)**
	2-3 to Disable SCSI terminator
JP5201	1-2 to enable SCSI terminator auto-enable mode.
	2-3 to disable SCSI terminator auto-enable mode **(Default)**
JP5301	1-2 to bypass VMEbus Interface in the JTAG scan chain **(Default)**

Table 4-12. **I/O Board Jumper Configurations**

Jumper ID	Description
	2-3 to include the VMEbus Interface in the JTAG scan chain
JP5302	2-3 Disable incoming SYSRESET* froim VMEbus
	1-2 Enable incoming SYSRESET* from VMEbus

a. For more information on manual ethernet port selection please contact Themis Customer Support.

The following table provides the jumper setting selecting access to the Boot FLASH. All other combinations are illegal.

Table 4-13. **Boot FLASH access**

Status	JP5102	JP5101
Normal Operation with access to Boot FLASH Devices (**Default**)	1-2	2-3
Update Boot FLASH, boot from ROMBO Connector	2-3	1-2

4.2.2.4 Flash Device Jumpers

The USP-1 uses Flash Devices. Flash Devices permit the following:

- Reprogramming of specific code blocks;
- Remote reprogramming of the FLASH chip by a system administrator over a local area network.

Table 4-14. Flash PROM Jumper setting

Default Jumper	Pins 1 + 2 Select	Pins 2 + 3 Select	Default Jumper Setting
J2002	Flash PROM	Not to Be Used	1-2
J2003	Write Protect	Write Enable	1-2
J2204	High Half Booting	Normal Booting	2-3

Note — If you are reprogramming your system FLASH, after successful reprogramming be sure to return the FLASH Write Protect/Enable jumper (J2003) to the Write Protect position to ensure system security.

For flash PROM reprogramming information and the function of J2204, see the *SMCC System Flash PROM Programming Guide.*

4.2.2.5 Serial Port Jumpers

The serial port jumpers on the I/O board permit configuring the TTY A and B line drivers for either EIA-423-A or EIA-232-A signal levels. EIA-423-A levels are the default standard for North American users. EIA-232-A levels are required for digital telecommunication in nations of the European Community.

Table 4-15. Serial Port Jumper Settings

Jumper	Pins 1 + 2	Pins 2 + 3	Default Jumper Setting
J2104	EIA-232 (High Threshold)	EIA-423 / EIA-232	2-3
J2105	EIA-232 (High Threshold)	EIA-423 / EIA-232	2-3

Note — Unless the receivers are high threshold receivers, the physical interface levels to EIA-423-A are compatible with most EIA-232-E receivers.

4.2.3 Jumper Locations

Pin 1 is identified with either an asterisk, number, or block.

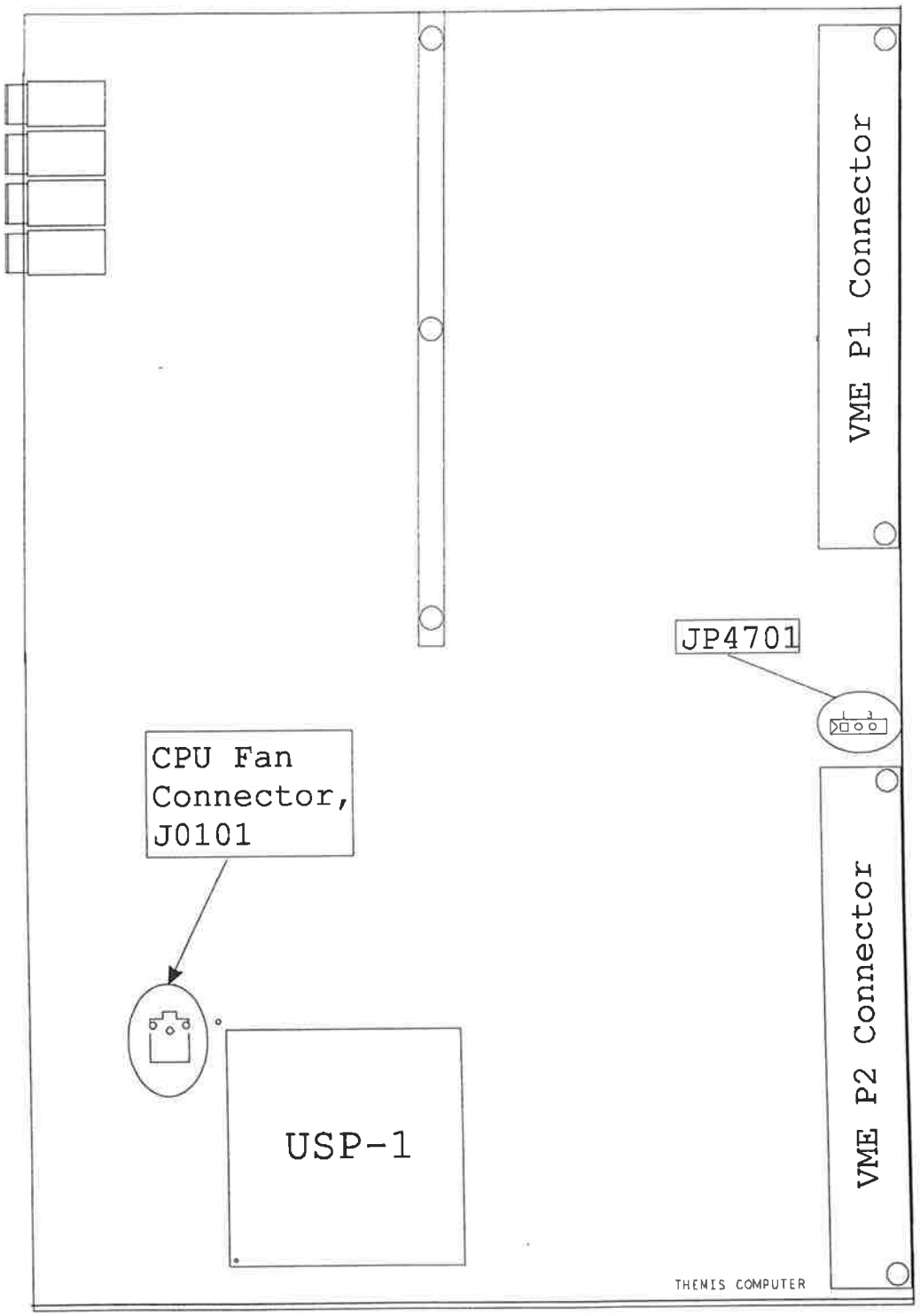


Figure 4-3. **Component Side: CPU Board Jumper Location**

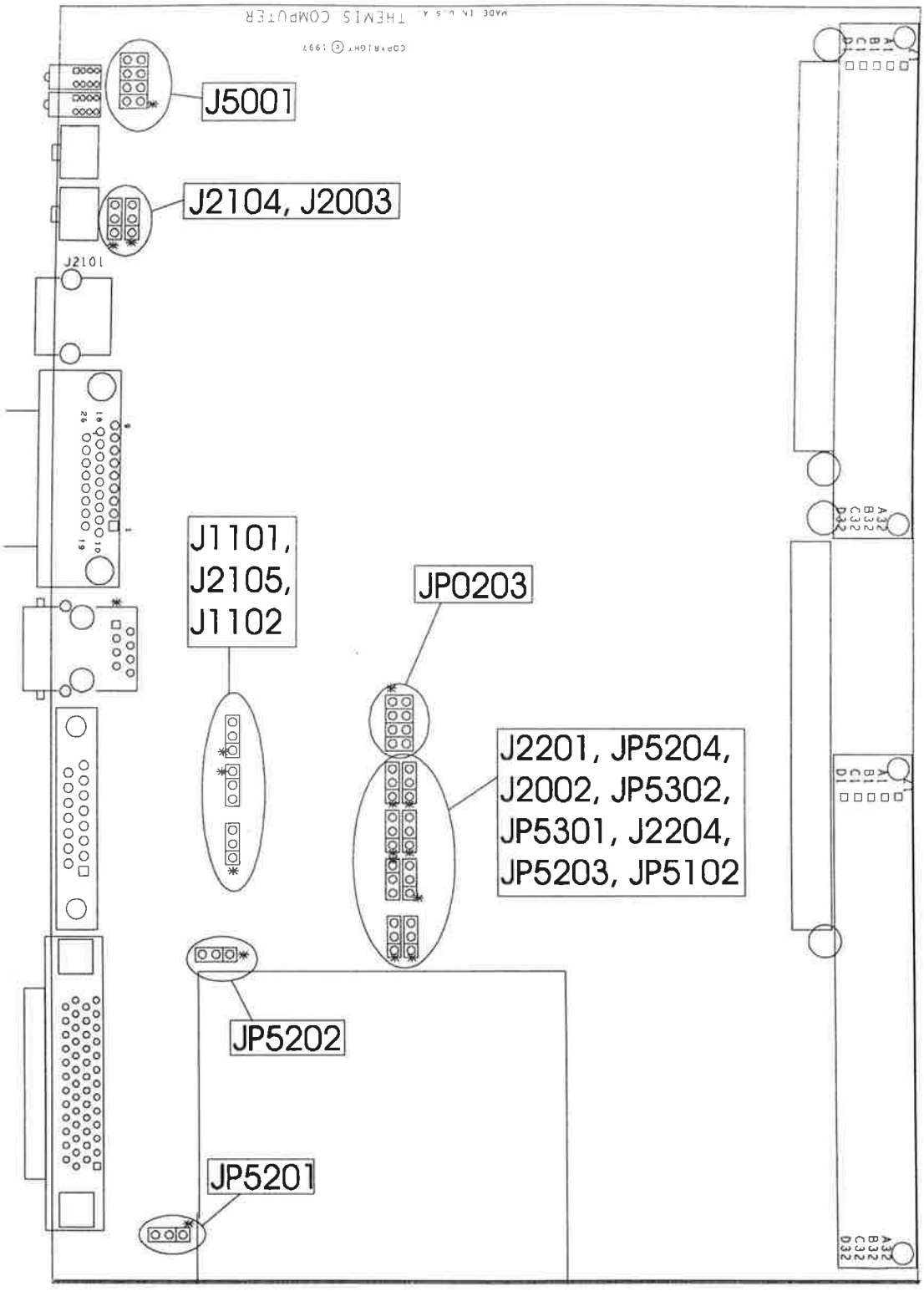


Figure 4-4. **Component Side: I/O Board Jumper Locations**

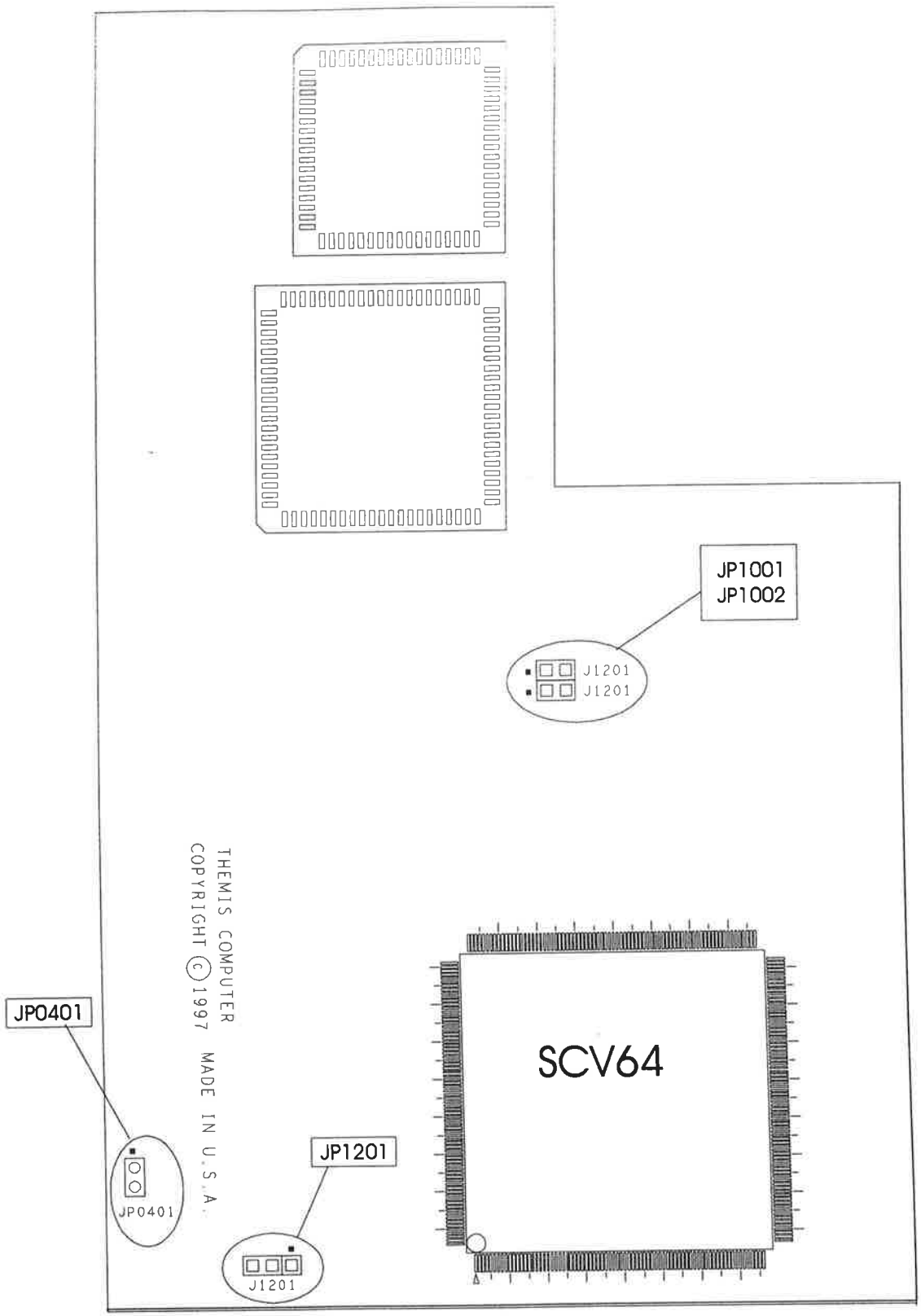


Figure 4-5. **Component Side: VSIC Board Jumper Locations**

This chapter describes these USP-1 specifications:

- Hardware and performance specifications
- Electrical power specifications
- Environmental specifications.

5.1 Hardware and Performance Specifications

Table 5-1 lists the USP-1 hardware and performance specifications

Table 5-1. USP-1 Hardware and Performance Specifications

Description	Specification
Physical Dimensions	
CPU Board Size	6U
Long Axis / Hort axis / Back panel height	3 Slot: 10.309 X 2.386
	4 Slot: 10.309x3.186
CPU Performance	
Estimated SPECint95 Performance	322 / 200 MHz
Estimated SPECfp95 Performance	7.44 /200 MHz
Estimated SPECfp95 Performance	10.4 / 462 MHz
Input / Output	
SBus Devices	Five Master / Slave devices
SBus Slots	Two physical slots
SBus Standard	SBus specifications, IEEE 1496 - 1993
SBus Data Size	64-Bit Full Master / Slave
Sbus Clock Rate	25MHz
SBus Write Sizes	Maximum 64-byte burst
Sbus Writes	64/32/16/8-byte burst mode supported

Table 5-1. USP-1 Hardware and Performance Specifications

Description	Specification
SCSI #2	A 50-pin, high density connector, located on the Paddle Board via P2 (CPU).
SCSI #1	A 50-pin, high density connector located on the front panel or on the Paddle Board via the P2 (I/O).
SCSI Standard	ANSI X3.133
SCSI Types	Synchronous / Asynchronous FAST Narrow
SCSI Performance	Up to 10 Mbyte per second (synchronous)
Ethernet #1 Connectors	RJ-45 jack for 10Base-T (twisted-pair) or AUI standard connector (DB-15) on the Front Panel and an AUI standard connector on the Paddle Board via P2 (I/O)
Ethernet #2 Connectors	AUI standard connector on the Paddle Board via P2 (CPU)
Ethernet Channels	#1 may be either thick AUI or twisted-pair.
	#2 is AUI only.
Ethernet Standard	IEEE 802.3
Printer (Parallel)	DB-25 Connector on the Paddle Board via P2 (I/O)
Printer Standards	IEEE 1284
Serial A/B Ports	One 26-pin D-Sub
Serial Standard	EIA-232-E / EIA-423-A
Serial Types	Synchronous / Asynchronous
Serial Configuration	DTE
Serial Performance	19,200 (19.2-Kbit) baud Hardware to 76.8 Kbaud Solaris to 38.4 Kbaud
Keyboard / Mouse Port	8-pin mini-circular jack
Floppy Diskette Drive (Intel 82077 compatible)	34-pin ribbon connector
Audio Headphone	Audio jack connector (stereo) (EIA standard 3.5mm/0.125" jacks)
Audio Line Out	Audio jack connector (stereo) (EIA standard 3.5mm/0.125" jacks)
Audio Line In	Audio Jack connector (stereo) (EIA standard 3.5mm/0.125" jacks)
Audio Microphone In	Audio connector (stereo) (EIA standard 3.5mm/0.125" jacks)
Audio Performance	Voice standard (8-bit, 8 Khz) and CD quality (16-bit, 48 Khz)
On-board Main Memory	

Table 5-1. USP-1 Hardware and Performance Specifications

Description	Specification
Description of Memory	Up to 2 Modules mounted on top of the CPU. Any combination of 128 MBytes and 256 MByte modules may be used.[a]
NVRAM / TOD Clock	8 KBytes
PROM	512 KBytes FLASH Memory
SBus	
SBus Controller Chip	U2S
SBus Connectors	2 Female SBus headers

a. Up to two (2), 256 MByte modules may be mounted on the bottom of the CPU. The 128 MByte modules cannot be mounted on the bottom of the stack.

5.2 Environmental Specifications

Table 3-3 and Table 3-4 contain the environmental specifications for the USP-1 under operating and non-operating conditions.

When measuring the operating environment air temperature for the USP-1, measure the air temperature as close to the air intake port on the enclosure as possible.

For cooling purposes, maximum air flow should be across the USP-1 board processor section, including the UltraSPARC processor, external cache SRAMS, and UDBs.

Table 5-2. USP-1 Operating Environmental Specifications

Description	Minimum Value	Maximum Value
Temperature Range	32 F (0 C)	104 F (50 C)
Humidity Range (relative non-condensing at 104 F (40 C)	5%	95%
Wet Bulb Maximum	Not applicable	77 F (25 C)
Altitude Range	0 feet (0 meters)	9,843 feet (3,000meters)
Air Flow	300 lfm airfow at 50 C	

Table 5-3. USP-1 Non-operating Environmental Specifications

Description	Minimum Value	Maximum Value
Temperature Range	32 F (0 C)	104 F (50 C)
Humidity Range (relative non-condensing at 104 F (40 C)	5%	95%
Wet Bulb Maximum	Not applicable	115 F (46 C)
Altitude Range	0 feet (0 meters)	38,370 feet (12000 meters)

6.1 Board Diagrams

This section presents general board and panel diagram for the USP-1.

6.1.1 Front Panels

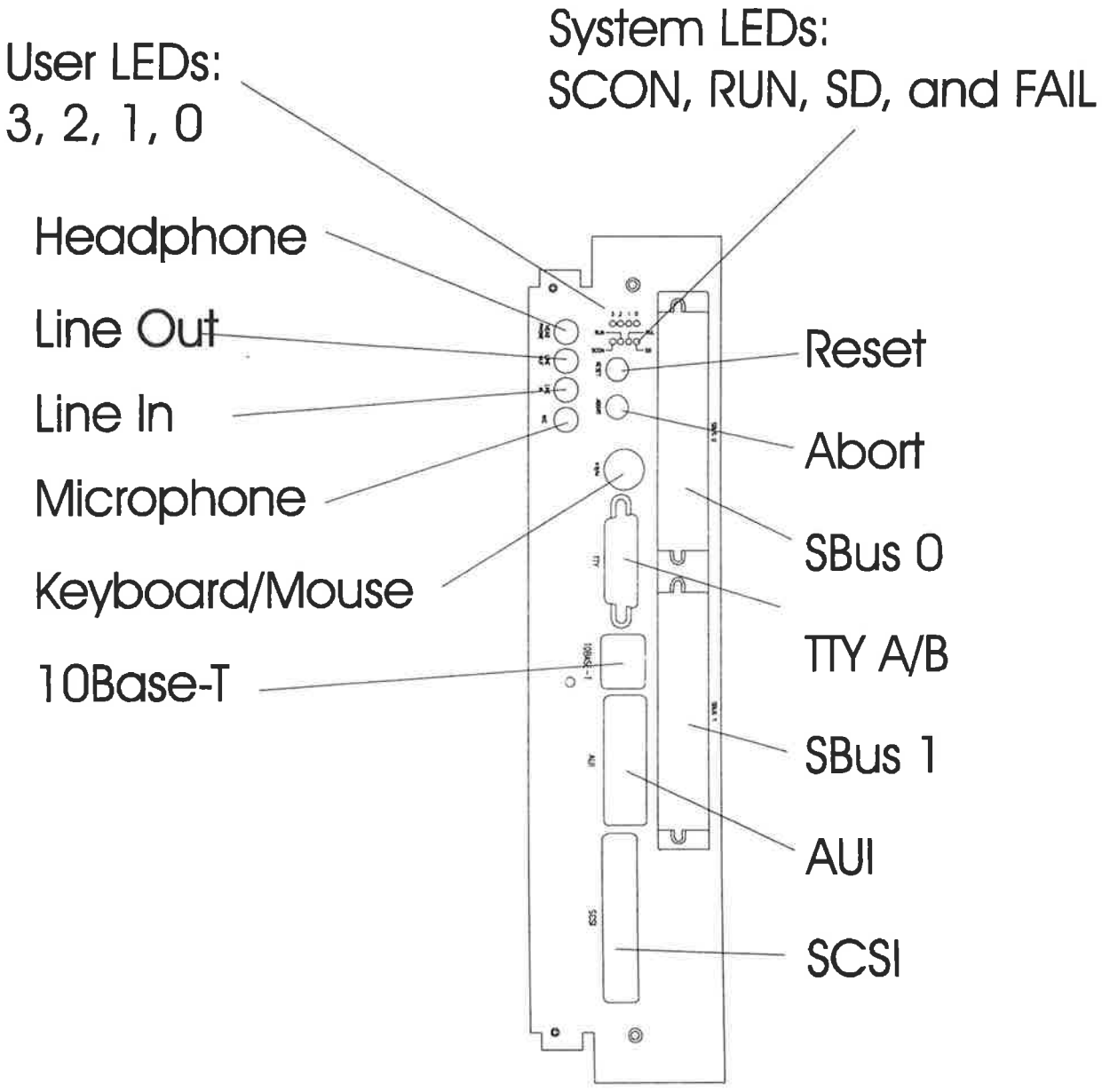


Figure 6-1. **Triple Slot Front Panel**

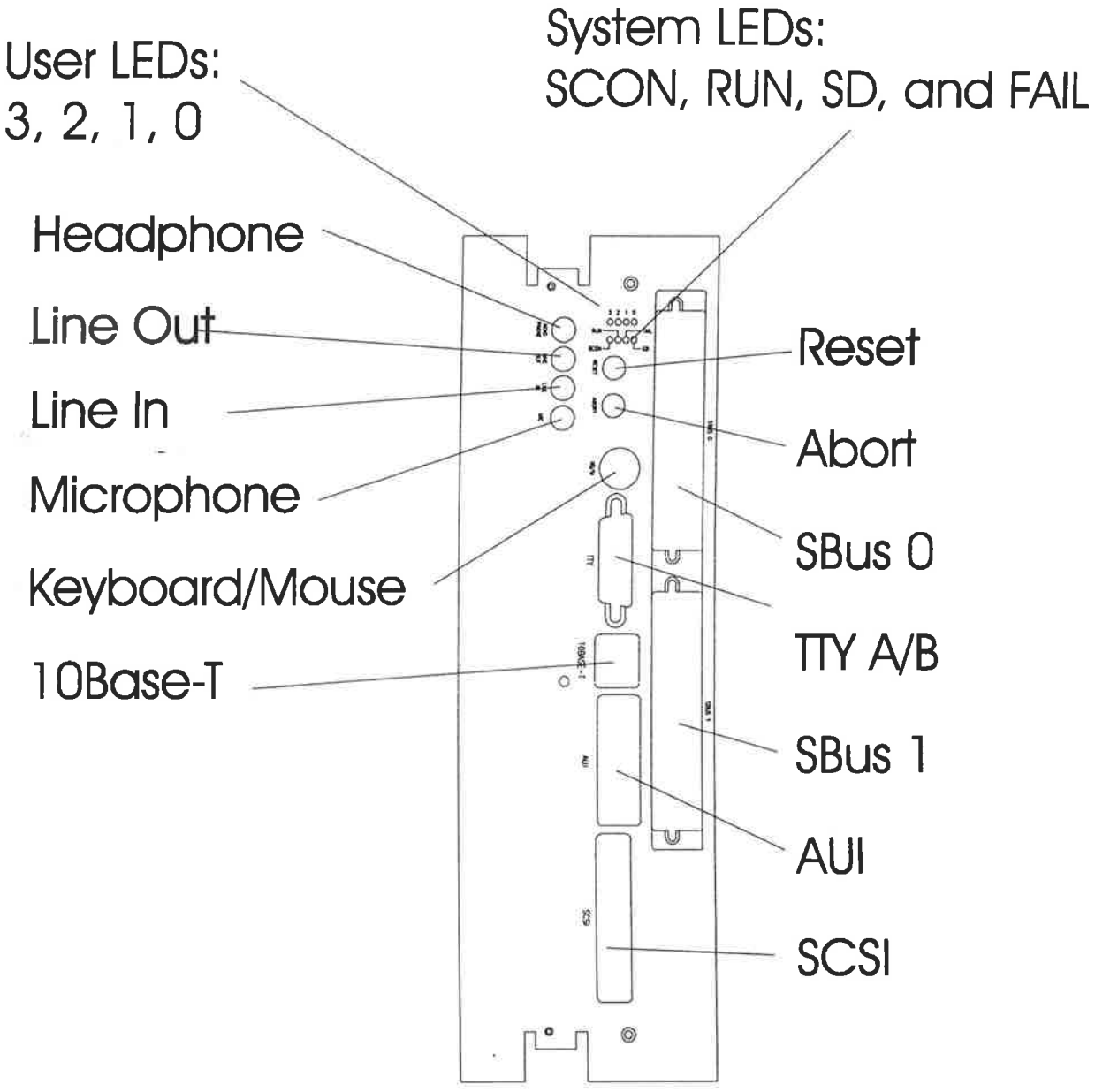


Figure 6-2. **Four Slot Front Panel**

6.1.2 Paddle Board

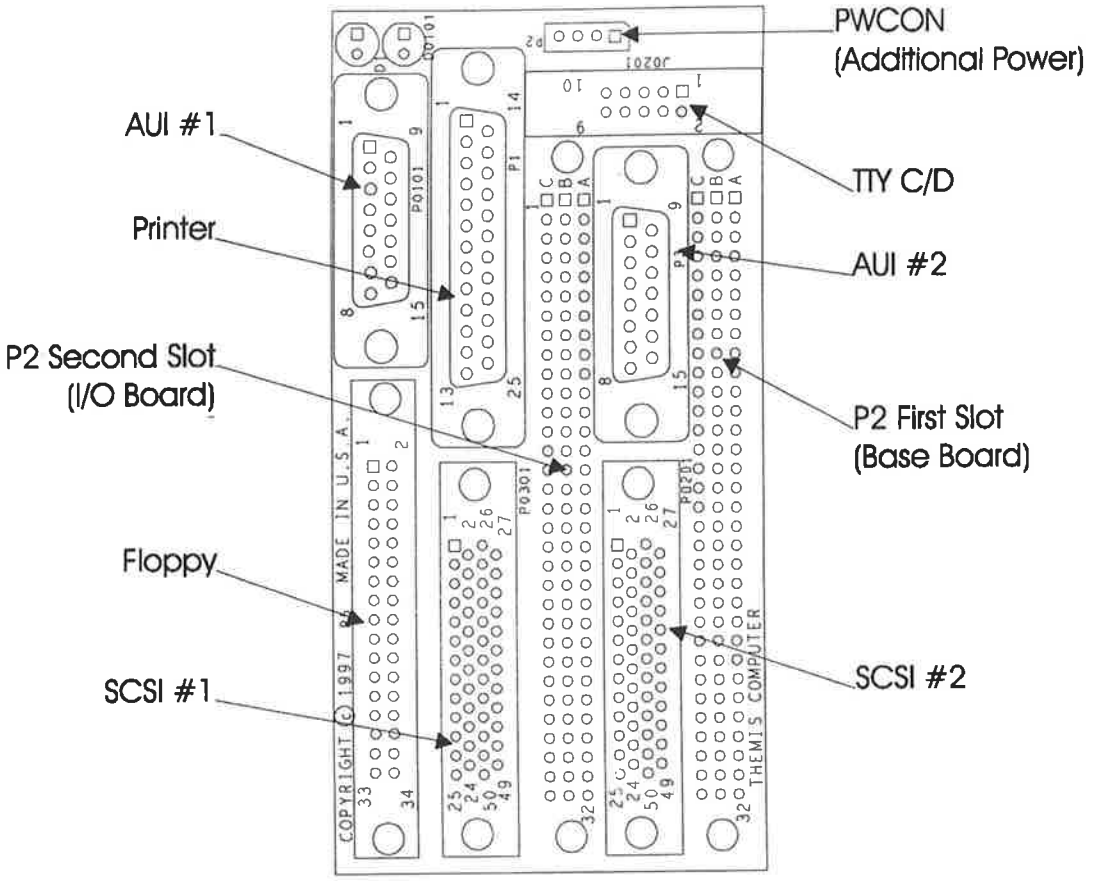


Figure 6-3. **Paddle Board**

6.1.3 CPU Board

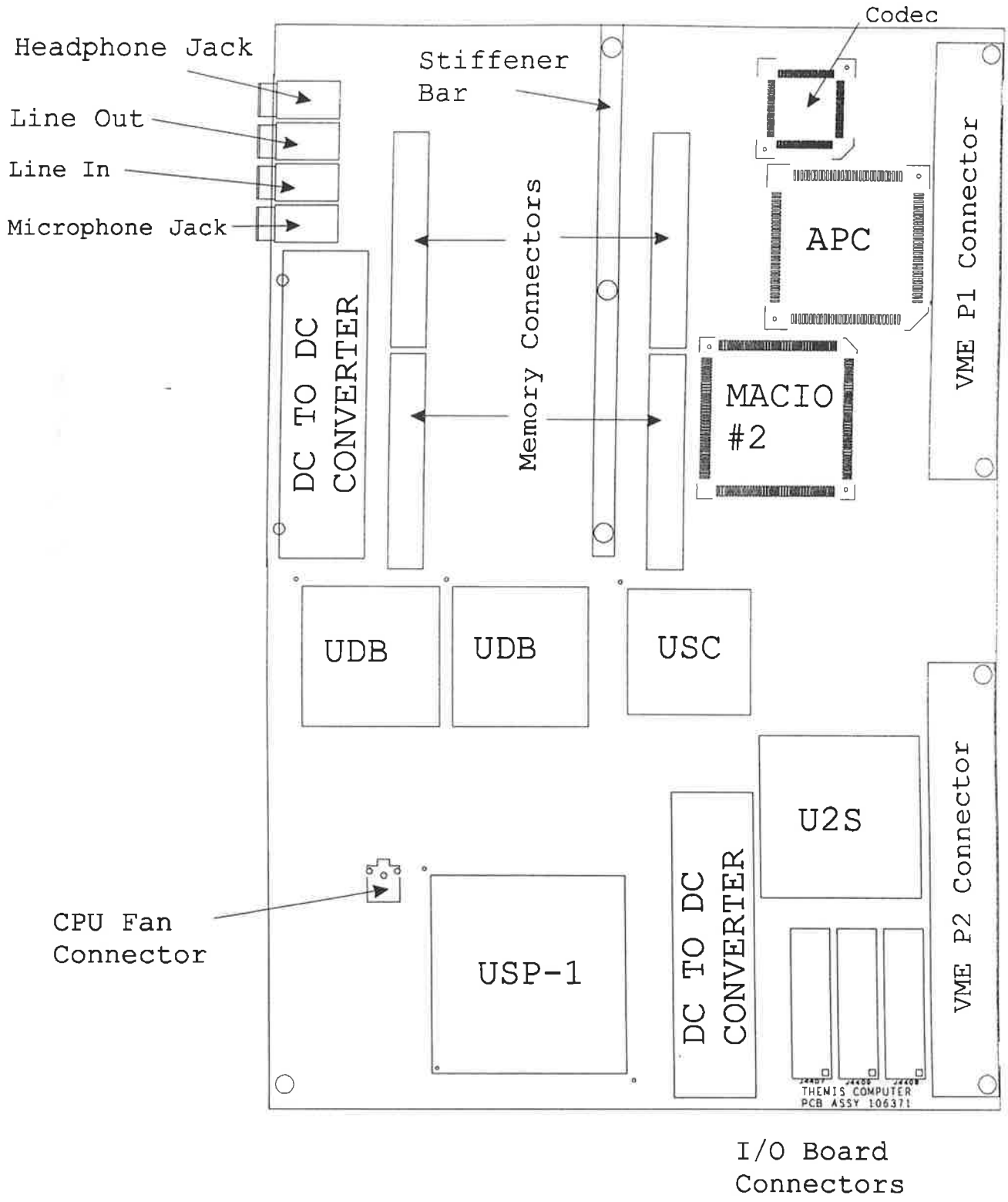


Figure 6-4. **CPU Board: Component Side**

6.1.4 VSIC Board

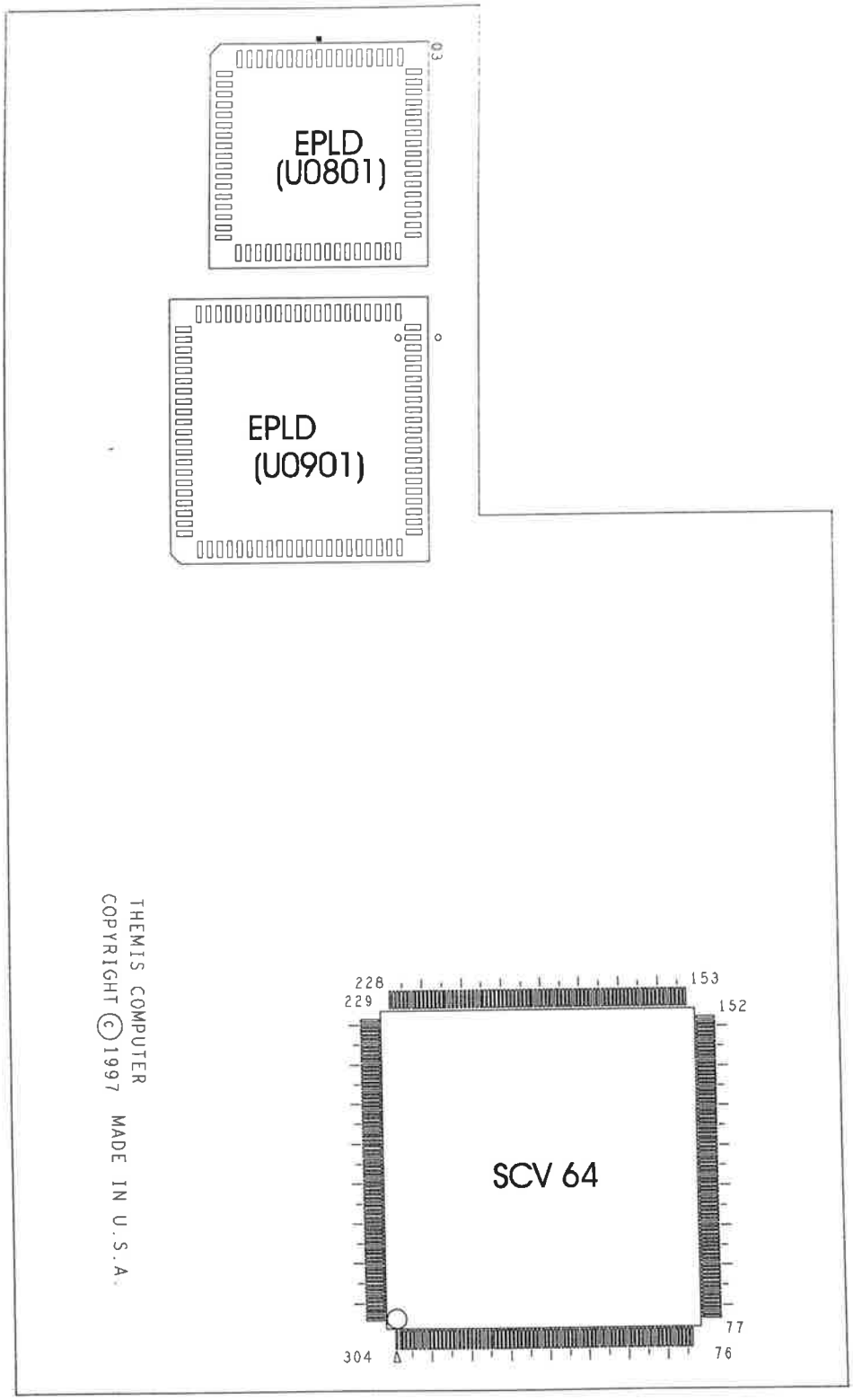


Figure 6-5. **VSIC Board: Component Side**

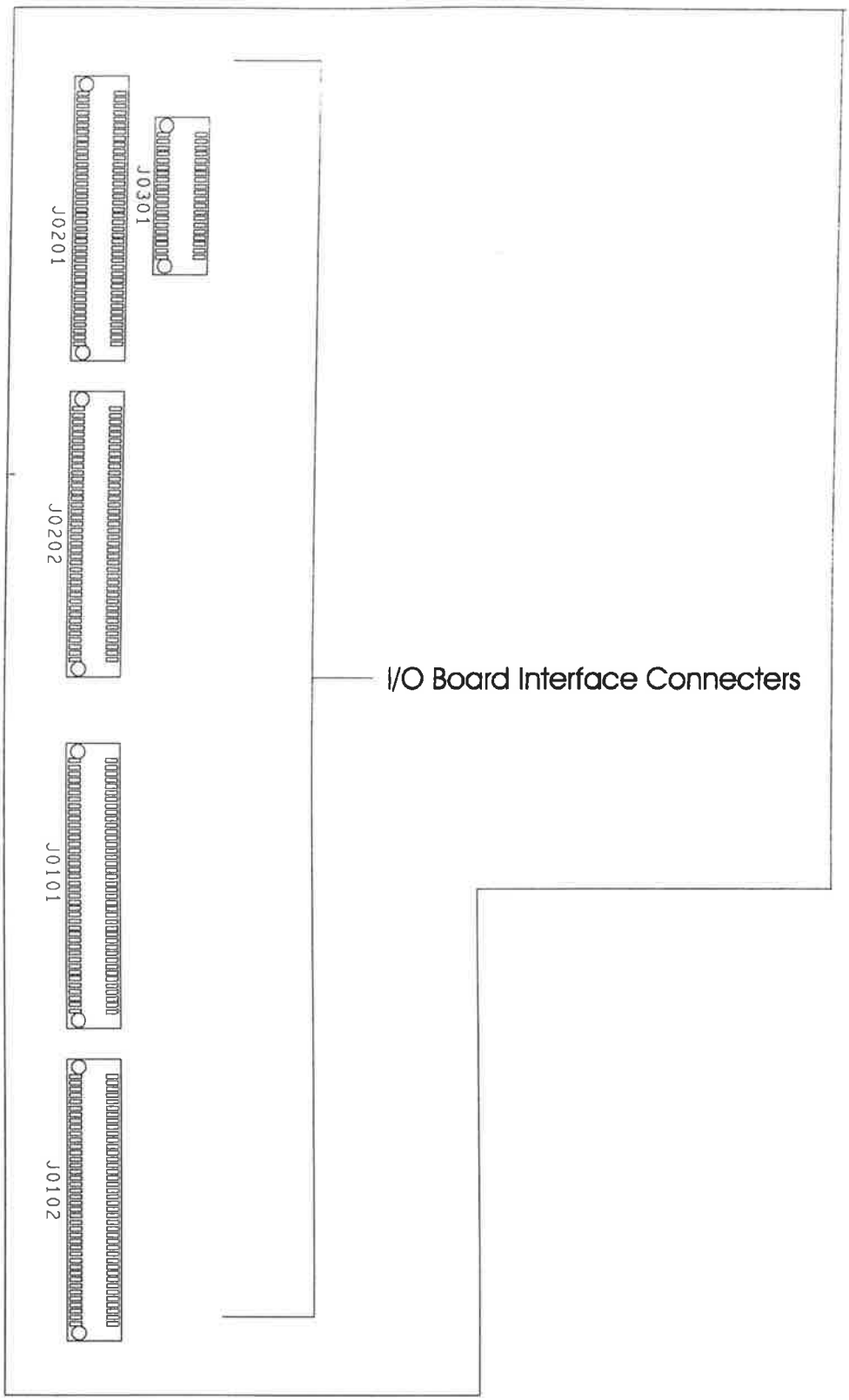


Figure 6-6. **VSIC Board: Solder Side**

6.1.5 I/O Board

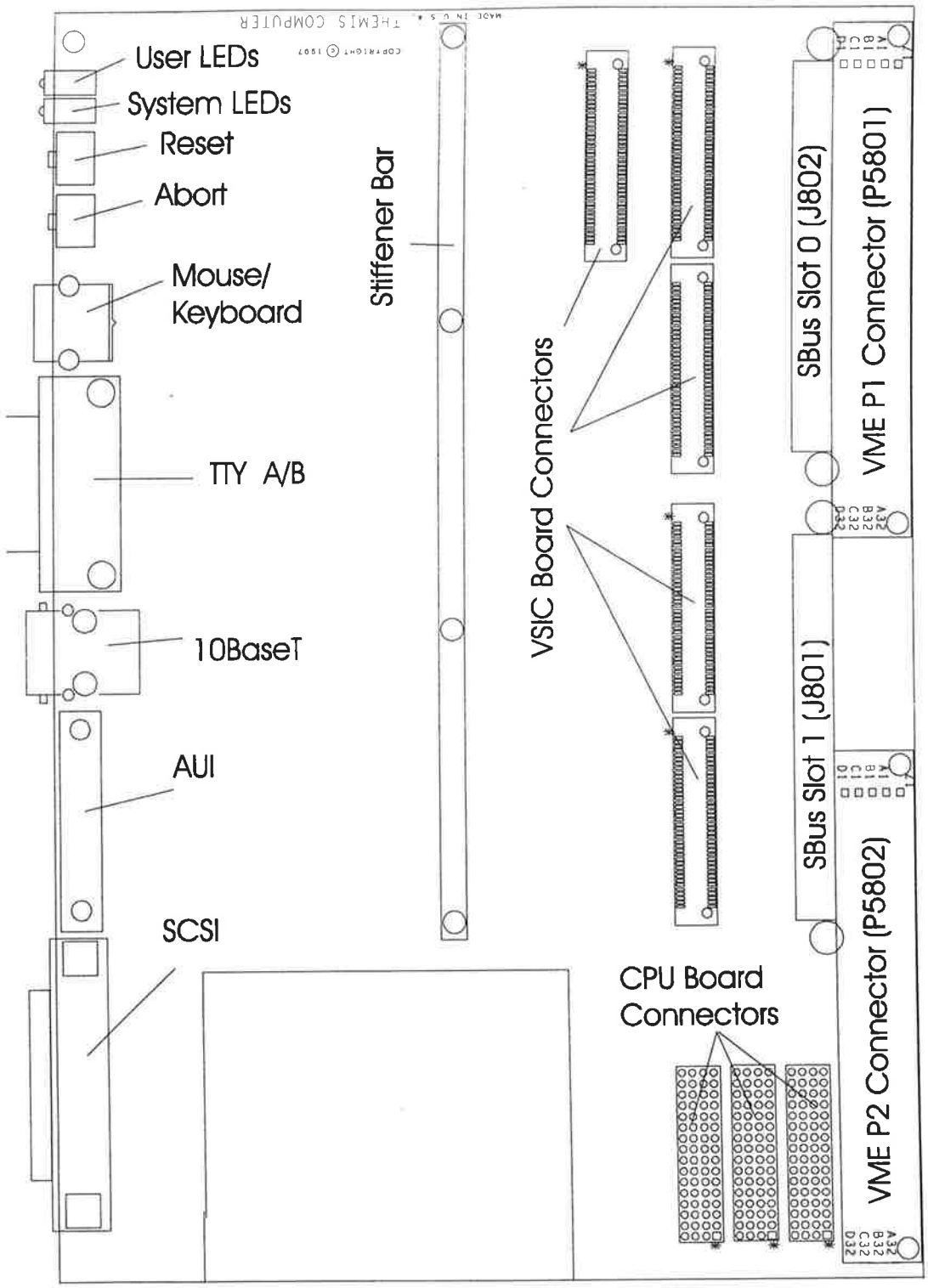


Figure 6-7. **I/O Board: Component Side**

6.1.6 Memory Boards

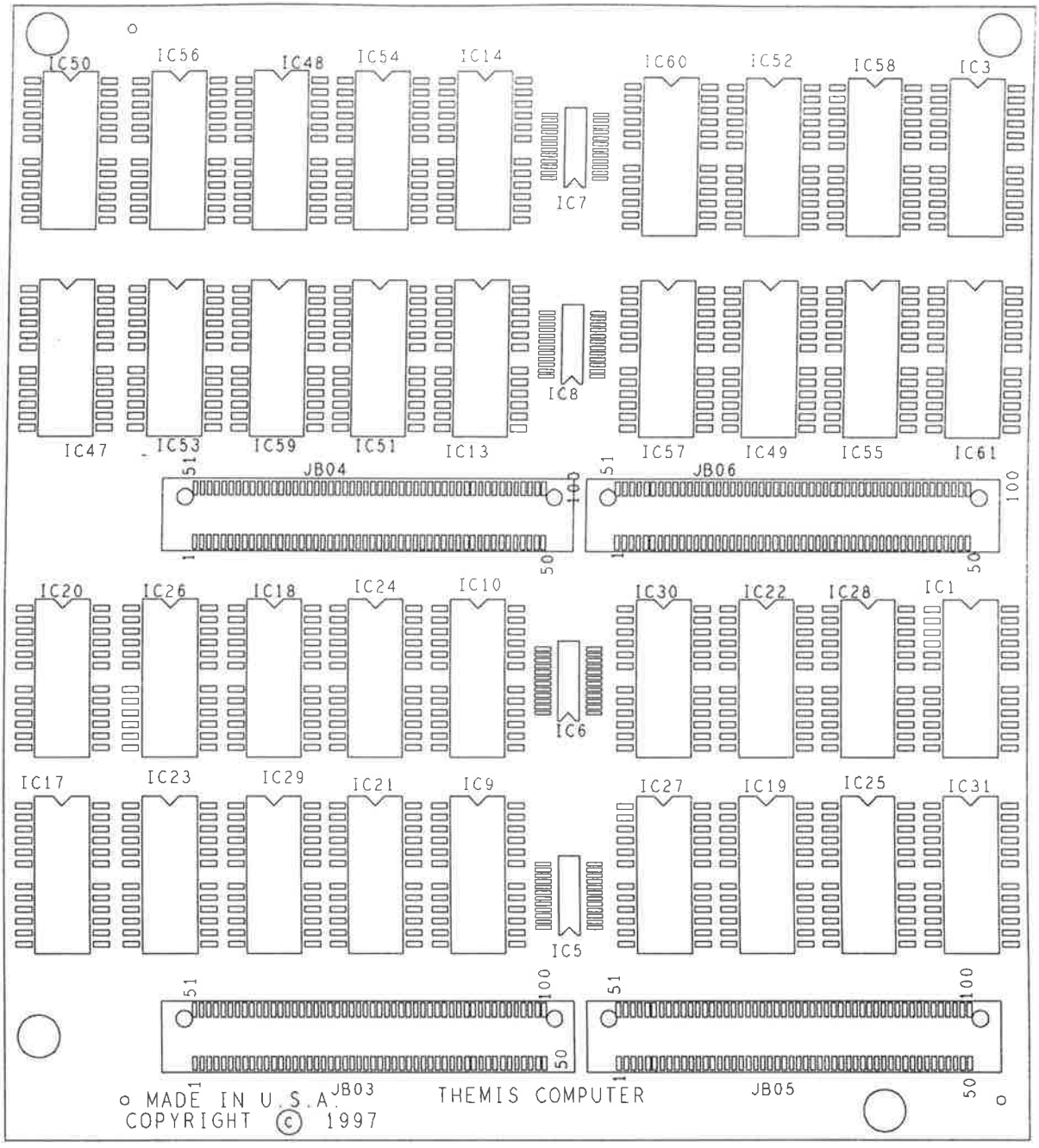


Figure 6-8. **128 MByte Memory Board: Component Size**

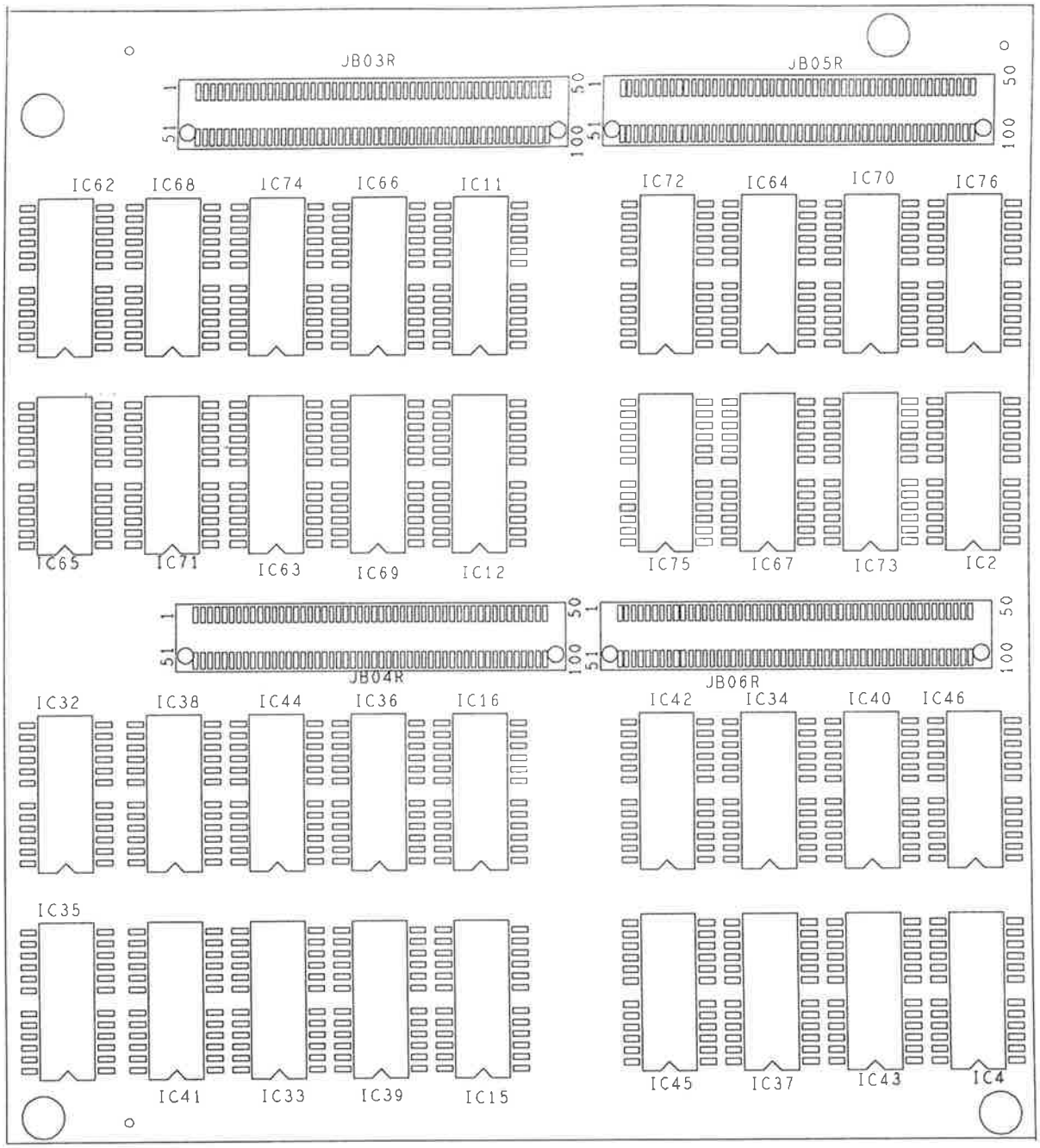


Figure 6-9. **128 MByte Memory Board: Solder Side**

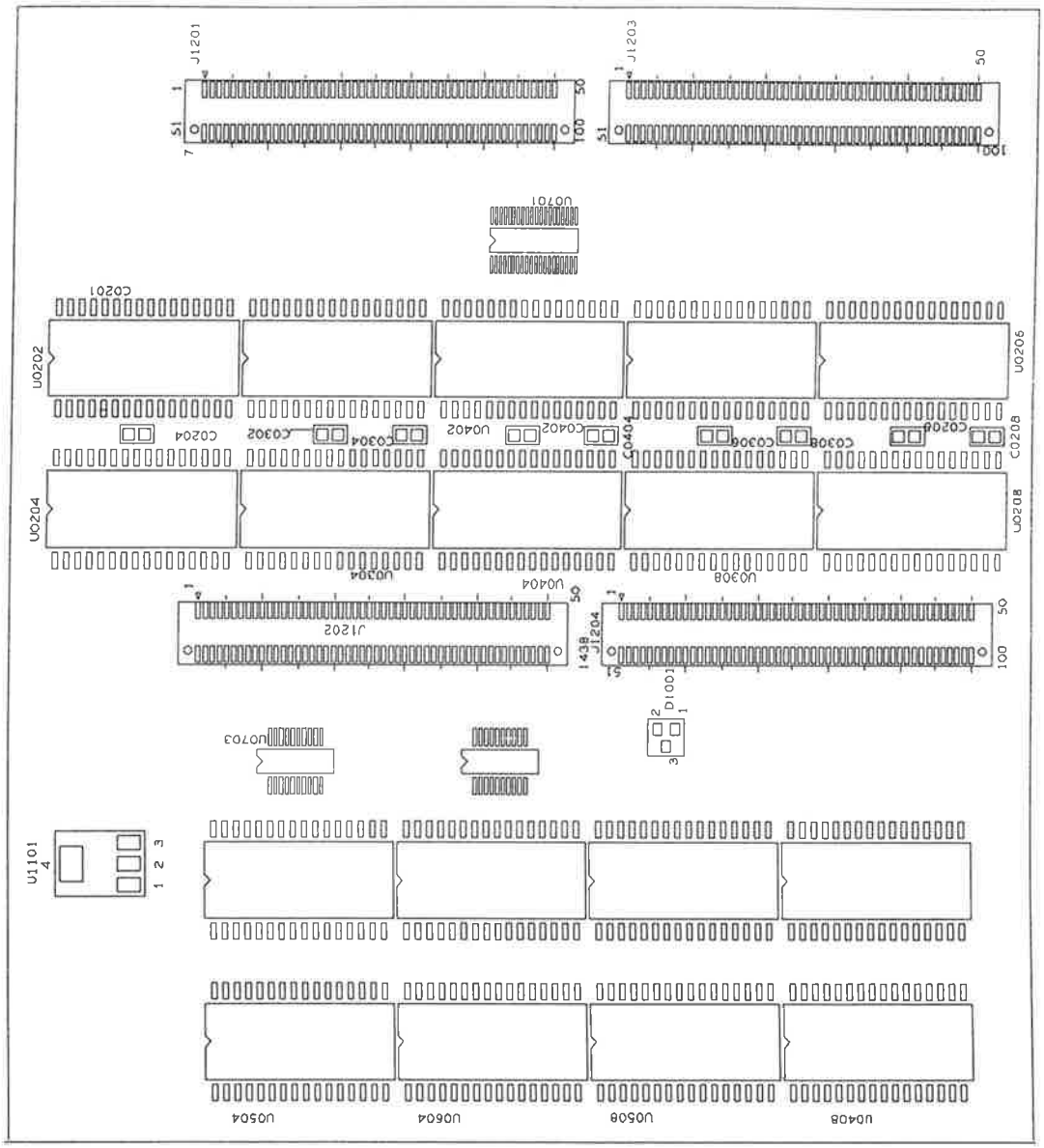


Figure 6-10. **256 MByte Memory Board: Component Side**

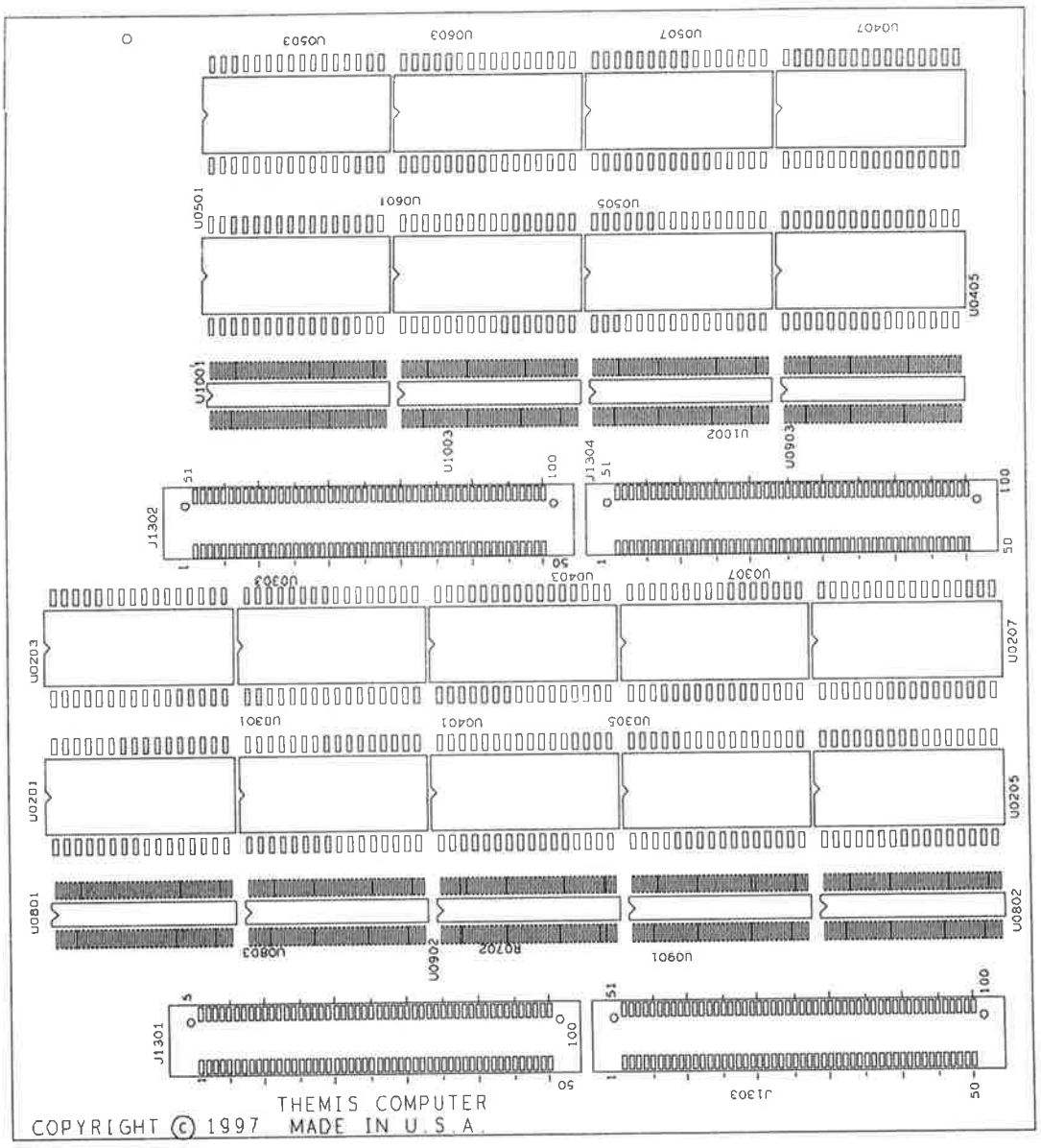


Figure 6-11. **256 MByte Memory Board: Solder Side**

7.1 Introduction

The USP-1 has various connectors located on the front panel, the baseboard (CPU Board), the I/O board, and the optional paddle board. Each of these connectors are listed below and described in a seperate section with illustrations and/or tables featuring a complete listing of the connector pinouts.

- **Front Panel Connectors**
  - TTY A/B (from the I/O Board)
  - Keyboard / Mouse (from the I/O Board)
  - AUI (from the I/O Board)
  - 10Base-T Ethernet (from the I/O Board)
  - SCSI (from the I/O Board)
  - Audio (from the CPU Board)
- **Base Board Connectors**
  - VMEbus P1 Connector
  - VMEbus P2 Connector
- **I/O Board Connectors**
  - VMEbus P1
  - VMEbus P2
  - SBus Connectors #1 and #2
- **Paddle Board Connectors**
  - SCSI (2)
  - TTY C/D
  - AUI Ethernet (2)
  - Parallel Port
  - Floppy Port

7.2 Front Panel Connectors

Described below are the connectors located on the front panel of the USP-1. Included are illustrations and/or tables featuring a complete listing of the connector pinouts. The views presented are taken while looking at the front panel.

7.2.1 TTY A/B Connector (Female)

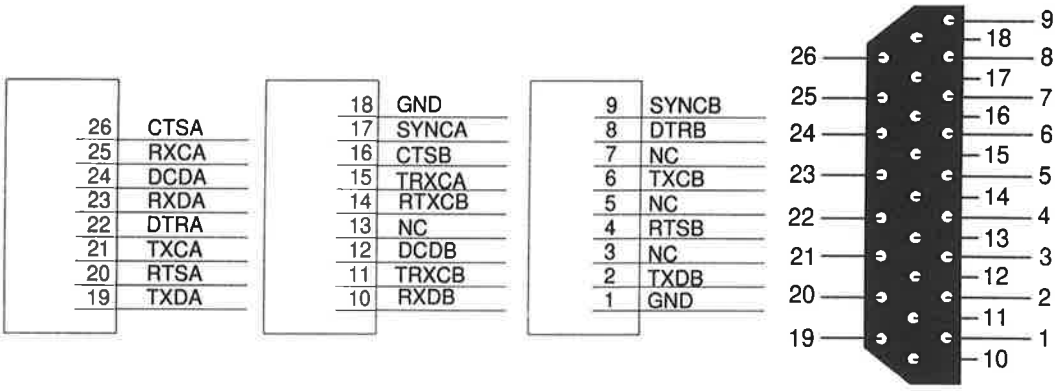


Figure 7-1. **Serial Ports A/B Connector Pinouts**

Table 7-1. **Serial Ports A/B Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1	GND	Ground		Ground
2	TXDB	Transmit Data B	Output	EIA232 / EIA423
3	NC	Not Connected		
4	RTSB	Request To Send B	Output	EIA232 / EIA423
5	NC	Not Connected		
6	TXCB	Transmit Clock B	Output	EIA232 / EIA423
7	NC	Not Connected		
8	DTRB	Data Terminal Ready B	Output	EIA232 / EIA423
9	SYNCB	Synchronization B	Input	EIA232 / EIA423
10	RXDB	Receive Data B	Input	EIA232 / EIA423
11	TRXCB	Transmit/Receive Clock B	Input	EIA232 / EIA423
12	DCDB	Data Carrier Detect B	Input	EIA232 / EIA423
13	NC	Not Connected		
14	RTXCB	Receive/Transmit Clock B	Input	EIA232 / EIA423
15	TRXCA	Transmit/Receive Clock A	Input	EIA232 / EIA423
16	CTSB	Clear To Send B	Input	EIA232 / EIA423

Table 7-1. **Serial Ports A/B Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction	Level
17	SYNCA	Synchronization A	Input	EIA232 / EIA423
18	GND	Ground A		Ground
19	TXDA	Transmit Data A	Output	EIA232 / EIA423
20	RTSA	Request To Send A	Output	EIA232 / EIA423
21	TXCA	Transmit Clock A	Output	EIA232 / EIA423
22	DTRA	Data Terminal Ready A	Output	EIA232 / EIA423
23	RXDA	Receive Data A	Input	EIA232 / EIA423
24	DCDA	Data Carrier Detect A	Input	EIA232 / EIA423
25	RTXCA	Receive/Transmit Clock A	Input	EIA232 / EIA423
26	CTSA	Clear To Send A	Input	EIA232 / EIA423

7.2.2 TTY A/B Serial Cable

An octopus adapter cable is provided by Themis to separate TTYA/B signals into standard TTYA and TTYB pinouts. The pinouts of the inputs and outputs to and from the cable is provided in this section. All connectors on the adapter cable are male. Also, the pins are individual labelled on the connectors. Note that the TTY A cable has a thinner diameter than the TTY B cable.

Figure 7-2. **TTY A/B Serial Adapter Cable Pinouts.**

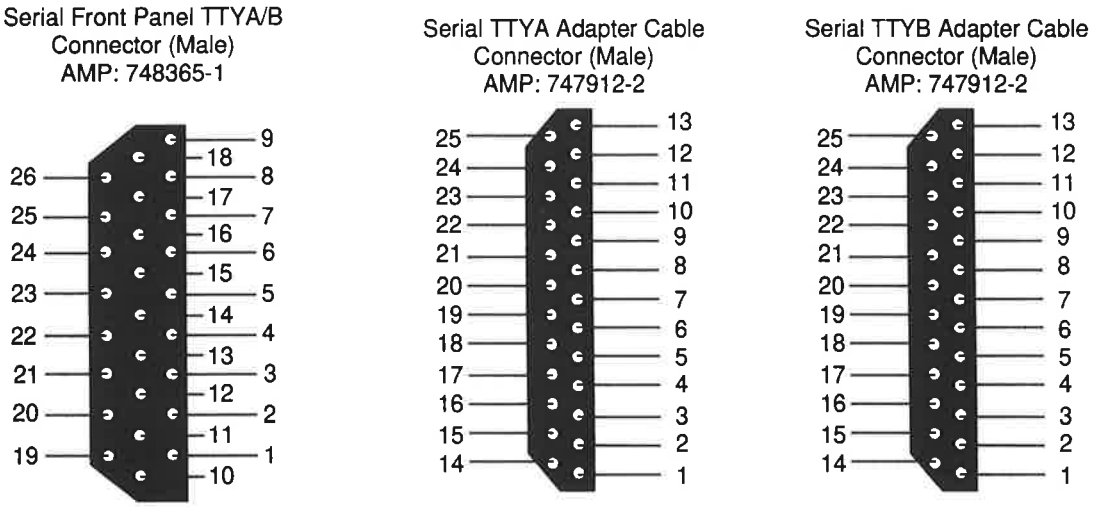


Table 7-2. **Serial Adapter Cable Pinout**

Front Panel Connector		TTY A Pin		TTY B Pin	
Pin	Signal	Pin	Signal	Pin	Signal
1	GND	--	--	7	GND
2	TXDB	--	--	3	TD_B+

Table 7-2. **Serial Adapter Cable Pinout**

Front Panel Connector		TTY A Pin		TTY B Pin	
Pin	Signal	Pin	Signal	Pin	Signal
3	NC	--	--	16	TD_B-
4	RTSB	--	--	5	RTS_B+
5	NC	--	--	18	RTS_B-
6	TXCB	--	--	24	TXC_B+
7	NC	--	--	12	TXC_B-
8	DTRB	--	--	8	DTR_B+
9	SYNCB	--	--	9	DTR_B-
10	RXDB	--	--	2	RD_B+
11	TRXCB	--	--	15	RD_B-
12	DCDB	--	--	20	DCD_B+
13	NC	--	--	21	DCD_B-
14	RTXCB	--	--	25	RXC_B+
15	TRXCA	--	--	13	RXC_B-
16	CTSB	--	--	4	CTS_B+
17	SYNCA	--	--	17	CTS_B-
18	GND	7	GND	--	--
19	TXDA	3	TD_A	--	--
20	RTSA	5	RTS_A	--	--
22	DTRA	8	DTR_A	--	--
23	RXDA	2	RD_A	--	--
24	DCDA	20	DCD_A	--	--
26	CTSA	4	CTS_A	--	--

7.2.3 Keyboard / Mouse Connector (Female)

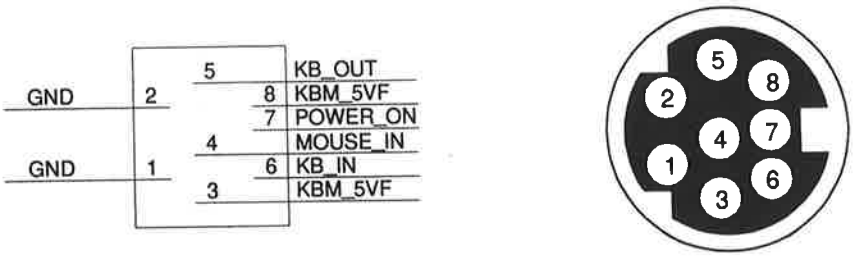


Figure 7-3. **Keyboard / Mouse Connector Pinouts**

Table 7-3. **Keyboard / Mouse Connector Pinouts**

Pin	Signal Name	Description	Direction
1	GND	Ground	--
2	GND	Ground	--
3	KBM_5VF	+5 VDC	Input
4	MOUSE_IN	Mouse in	Input
5	KB_OUT	Keyboard Out	Output
6	KB_IN	Keyboard In	Input
7	POWER_ON	RTC Alarm or Frequency Test	Output
8	KBM_5VF	+5 VDC	

7.2.4 Ethernet AUI #1 Connector (Female)

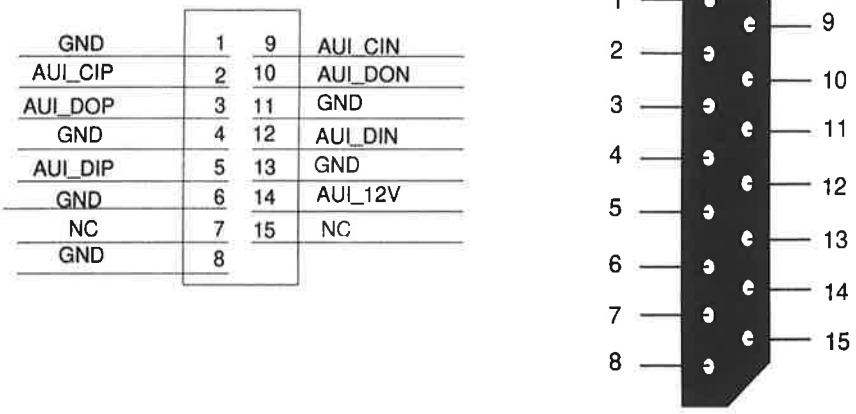


Figure 7-4. **AUI Ethernet Connector Pinouts**

Table 7-4. **AUI Ethernet Connector Pinouts**

Pin	Signal Name	Description	Direction
1	GND	Ground	
2	AUI_CIP	Collision (+)	Input
3	AUI_DOP	Transmit Data (+)	Output
4	GND	Ground	
5	AUI_DIP	Receive Data (+)	Input
6	GND	Ground	

Table 7-4. **AUI Ethernet Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction
7	NC	Not Connected	
8	GND	Not Connected	
9	AUI_CIN	Collision (-)	Input
10	AUI_DON	Transmit Data (-)	Output
11	GND	Ground	
12	AUI_DIN	Receive Data (-)	Input
13	AUI_12v	+12V	
14	NC	Not Connected	
15	NC	Not Connected	

7.2.5 10Base-T Ethernet Connector

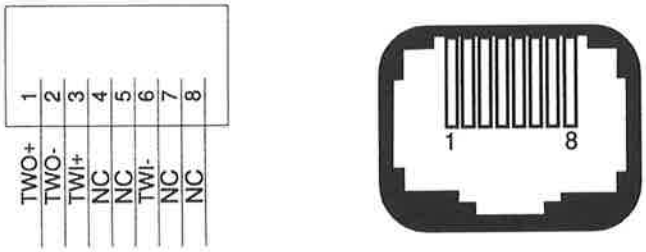


Figure 7-5. **10Base-T Ethernet Connector Pinouts**

Table 7-5. **10Base-T Ethernet Connector Pinouts**

Pin	Signal Name	Description	Direction
1	TWO+	Transmit Data (+)	Output
2	TWO-	Transmit Data (-)	Output
3	TWI+	Receive Data (+)	Input
4	NC	Not Connected	
5	NC	Not Connected	
6	TWI-	Receive Data (-)	Input
7	NC	Not Connected	
8	NC	Not Connected	

7.2.6 SCSI #1 Connector (Female, High Density)

SCSI_IO*	50	25	GND
SCSI_REQ*	49	24	GND
SCSI_CD*	48	23	GND
SCSI_SEL*	47	22	GND
SCSI_MSG*	46	21	GND
SCSI_RST*	45	20	GND
SCSI_ACK*	44	19	GND
SCSI_BSY*	43	18	GND
GND	42	17	GND
SCSI_ATN*	41	16	GND
GND	40	15	GND
GND	39	14	GND
TERMPWR+	38	13	FRONT_SCSI*
GND	37	12	GND
NC	36	11	GND
GND	35	10	GND
SCSI_PAR0	34	9	GND
SCSI_D7	33	8	GND
SCSI_D6	32	7	GND
SCSI_D5	31	6	GND
SCSI_D4	30	5	GND
SCSI_D3	29	4	GND
SCSI_D2	28	3	GND
SCSI_D1	27	2	GND
SCSI_D0	26	1	GND

Figure 7-6. **SCSI #1 Connector Pinouts**

Table 7-6. **SCSI #1 Connector Pinouts**

Pin	Signal Name	Description	Direction
1	GND	Ground	
2	GND	Ground	
3	GND	Ground	
4	GND	Ground	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	FRONT_SCSI*	SCSI #1 Auto Sense - Front Panel	Input
14	GND	Ground	
15	GND	Ground	

Table 7-6. **SCSI #1 Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction
16	GND	Ground	
17	GND	Ground	
18	GND	Ground	
19	GND	Ground	
20	GND	Ground	
21	GND	Ground	
22	GND	Ground	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	SCSI_D0	Data Bit	Input / Output
27	SCSI_D1	Data Bit	Input / Output
28	SCSI_D2	Data Bit	Input / Output
29	SCSI_D3	Data Bit	Input / Output
30	SCSI_D4	Data Bit	Input / Output
31	SCSI_D5	Data Bit	Input / Output
32	SCSI_D6	Data Bit	Input / Output
33	SCSI_D7	Data Bit	Input / Output
34	SCSI_PAR0	Data Parity Bit	Input / Output
35	GND	Ground	
36	NC	Not Connected	
37	GND	Ground	
38	TERMPWR+	Termination Voltage	
39	GND	Ground	
40	GND	Ground	
41	SCSI_ATN*	Attention	Output
42	GND	Ground	
43	SCSI_BSY*	Busy	Output
44	SCSI_ACK*	Acknowledge	Output
45	SCSI_RST*	Reset	Output
46	SCSI_MSG*	Message	Output
47	SCSI_SEL*	Select	Output
48	SCSI_CD*	Control / Data	Output
49	SCSI_REQ*	Request	Output
50	SCSI_IO*	Input / Output	Output

7.2.7 Audio Ports

All Audio Ports use EIA standard 3.5mm / .0125-inch jacks.

Table 7-7. Audio Port Signals

	Headphone	Line Out	Line in	Microphone
Tip	Left Channel	Left Channel	Left Channel	Left Channel
Ring(Center)	Right Channel	Right Channel	Right Channel	Right Channel
Shield	Ground	Ground	Ground	Ground

Table 7-8. Audio Port Functions

Port	Function
Headphones	Connects stereophonic headphones for private listening of audio output.
Line Out	Connects the system audio output to an external sterophonic amplifier and loudspeakers.
Line In	Connects external sterophonic audio sources such a compact disc player or cassette tape player to the system.
Microphone	Connects the SunMicrophone II (or other suitable microphone*) to the system.

TheSPARCstation 11 microphone port accepts stereophonic input: however, the Sun Microphone II is a monophonic device. Note that the older SunMicophone in not compatible with the SPARCstation 11 system.

7.2.7.1 Audio Specifications

The specifications below assume use of the Audio Tool format setting "CD-ROM" or "DAT" has been selected.

The microphone input specifications are for the SunMicrophone II.

Table 7-9. Audio Inputs and Output

Stereo	Specifications
Line In	2V typical, 4V max.; 5-50 ohm impedance
Frequency Response	20 Hz- 17 kHz +/-0.5 dB
Internal CD Input	
Input Level	0.1 Vrms typical at 10 kohm; 2Vpp max.
Distortion	0.01%, typical at 1kHz
S/N Ratio	84 dB, typical IEC 179 A-weighted
Frequency Response	20 Hz-17 kHz +/-0.5 dB

Table 7-9. Audio Inputs and Output

Stereo	Specifications
Microphone Input	15mV typical, 0.6-1.0 kohm impedance; +5 VDC input bias via a 2.2 kohm resistor
Headphones Output	1V typical, 2.4V max.; 16ohm- 1 kohm impedance
Line Out	1V typical, 2.4V max.; 5-50 kohm impedance

7.3 Baseboard Connectors

Described below are the connectors located on the baseboard of the UPS-1. Included are illustrations and/or tables featuring a complete listing of the connector pinouts.

7.3.1 VMEbus P1 Connector (Base Board)

ROW A		ROW B		ROW C	
A1		B1		C1	
A2		B2		C2	
A3		B3		C3	
A4		B4	BGI0*	C4	
A5		B5	BGO0*	C5	
A6		B6	BGI1*	C6	
A7		B7	BGO1*	C7	
A8		B8	BGI2*	C8	
A9	GND	B9	BGO2*	C9	GND
A10		B10	BG13*	C10	
A11	GND	B11	BGO3*	(1) C11	
A12		B12		C12	
A13		B13		C13	
A14		B14		C14	
A15	GND	B15		C15	
A16		B16		C16	
A17	GND	B17		C17	
A18		B18		C18	
A19	GND	B19		C19	
A20		B20	GND	C20	
A21	IACKI*	B21		C21	
A22	IACKO*	B22		C22	
A23		B23	GND	C23	
A24		B24		C24	
A25		B25		C25	
A26		B26		C26	
A27		B27		C27	
A28		B28		C28	
A29		B29		C29	
A30		B30		C30	
A31	-12V	B31		C31	+12V
A32	+5V	B32	+5V	C32	+5V

Figure 7-7. **VMEbus P1 Connector Pinouts**

The following table contains signal description for the VMEbus P1 Baseboard connection. Unused connections are not included in the signal description.

Table 7-10. **VMEbus P1 Connector Description**

Pin	Signal Name	Description
A9	GND	Ground
A11	GND	Ground
A15	GND	Ground
A17	GND	Ground
A19	GND	Ground
A21	IACKI*	Interrupt Acknowledge In
A22	IACKO*	Interrupt Acknowledge Out
A31	-12V	
A32	+5V	
B4	BGIO*	
B5	BGO0*	
B6	BGI1*	
B7	BGO1*	
B8	BGI2*	
B9	BGO2*	
B10	BGI2*	
B11	BGI2*	
C9	GND	Ground
C31	+12V	
C32	+5V	

7.3.2 VMEbus P2 Connector (Base Board)

ROW A		ROW B		ROW C	
A1	+5V	B1	+5V	C1	+5V
A2	GND	B2	GND	C2	GND
A3	+5V	B3		C3	+3.3V
A4	+5V	B4		C4	+3.3V
A5	NC	B5		C5	NC
A6	TTY_C_RXD_L	B6		C6	TTY_D_RXD_L
A7	TTY_C_TXD_L	B7		C7	TTY_D_TXD_L
A8	+5V	B8		C8	+5V
A9	AUX_AUI_12V	B9		C9	+5V
A10	AUX_AUI_DI-	B10		C10	NC
A11	AUX_AUI_DI+	B11		C11	GND
A12	GND	B12	GND	C12	GND
A13	AUX_AUI_DO-	B13	+5V	C13	AUX_SCSI_D0
A14	AUX_AUI_DO+	B14		C14	AUX_SCSI_D1
A15	GND	B15		C15	AUX_SCSI_D2
A16	AUX_AUI_CI-	B16		C16	AUX_SCSI_D3
A17	AUX_AUI_CI+	B17		C17	AUX_SCSI_D4
A18	GND	B18		C18	AUX_SCSI_D5
A19	REAR_SCSI	B19		C19	AUX_SCSI_D6
A20	AUX_TERM_POWER	B20		C20	AUX_SCSI_D7
A21	GND	B21		C21	AUX_SCSI_PAR0
A22	AUX_SCSI_ATN_L	B22	GND	C22	GND
A23	AUX_SCSI_BSY_L	B23		C23	AUX_SCSI_CD_L
A24	AUX_SCSI_ACK_L	B24		C24	AUX_SCSI_REQ_L
A25	AUX_SCSI_RST_L	B25		C25	AUX_SCSI_IO_L
A26	AUX_SCSI_MSG_L	B26		C26	AUX_SCSI_SEL_L
A27	+5V	B27		C27	+5V
A28	+5V	B28		C28	+3.3V
A29	+5V	B29		C29	+3.3V
A30	+5V	B30		C30	+3.3V
A31	GND	B31	GND	C31	GND
A32	+5V	B32	+5V	C32	+5V

Figure 7-8. **VMEbus P2 Connector Pinouts**

The VMEbus P2 Connector accommodates user-defined signals. The optional paddleboard is one way of easily accessing the USP-1 VMEbus P2 Connector user-defined signals. The following table lists the VMEbus P2 Connector user-defined signals.

Table 7-11. **VMEbus P2 Connector Pinout of User-defined Signals**

Pin	Signal Name	Description	Direction
A1	+5V	+5V	
A2	GND	GND	
A3	+5V	+5V	
A4	+5V	+5V	
A5	NC	Not Connected	

Table 7-11. **VMEbus P2 Connector Pinout of User-defined Signals** (Continued)

Pin	Signal Name	Description	Direction
A6	TTY_C_RXD_L	TTYC Receive Data	Input
A7	TTY_C_TXD_L	TTYC Transmit Data	Output
A8	+5V	+5V	
A9	AUX_AUI_12V	AUI #2: +12V	
A10	AUI_DI-	AUI #2: Receive Data (-)	Input
A11	AUI_DI+	AUI #2: Receive Data (+)	Input
A12	GND	GND	
A13	AUX_AUI_DO-	AUI #2: Transmit Data (-)	Output
A14	AUX_AUI_DO+	AUI #2: Transmit Data (+)	Output
A15	GND	GND	
A16	AUX_AUI_CI-	AUI #2: Collision (-)	Input
A17	AUX_AUI_CI+	AUI #2:Collision (+)	Input
A18	GND	GND	
A19	REAR_SCSI	SCSI #2 Auto Sense	Input
A20	AUX_SCSI_TERM_POWER	SCSI #2 Termination Power	
A21	GND	GND	
A22	AUX_SCSI_ATN_L	SCSI #2 Attention	Output
A23	AUX_SCSI_BSY_L	SCSI #2 Busy	Input / Output
A24	AUX_SCSI_ACK_L	SCSI #2 Acknowledge	Output
A25	AUX_SCSI_RST_L	SCSI #2 Reset	Input / Output
A26	AUX_SCSI_MSG_L	SCSI #2 Message	Input
A27	+5V	+5V	
A28	+5V	+5V	
A29	+5V	+5V	
A30	+5V	+5V	
A31	GND	GND	
A32	+5V	+5V	
C1	+5V	+5V	
C2	GND	GND	
C3	+3.3V	+3.3V	
C4	+3.3V	+3.3V	
C5	NC	Not Connected	
C6	TTY_D_RXD_L	Receive TTYD Data	Input
C7	TTY_D_TXD_L	TTYD Transmit Data	Output
C8	+5V	+5V	

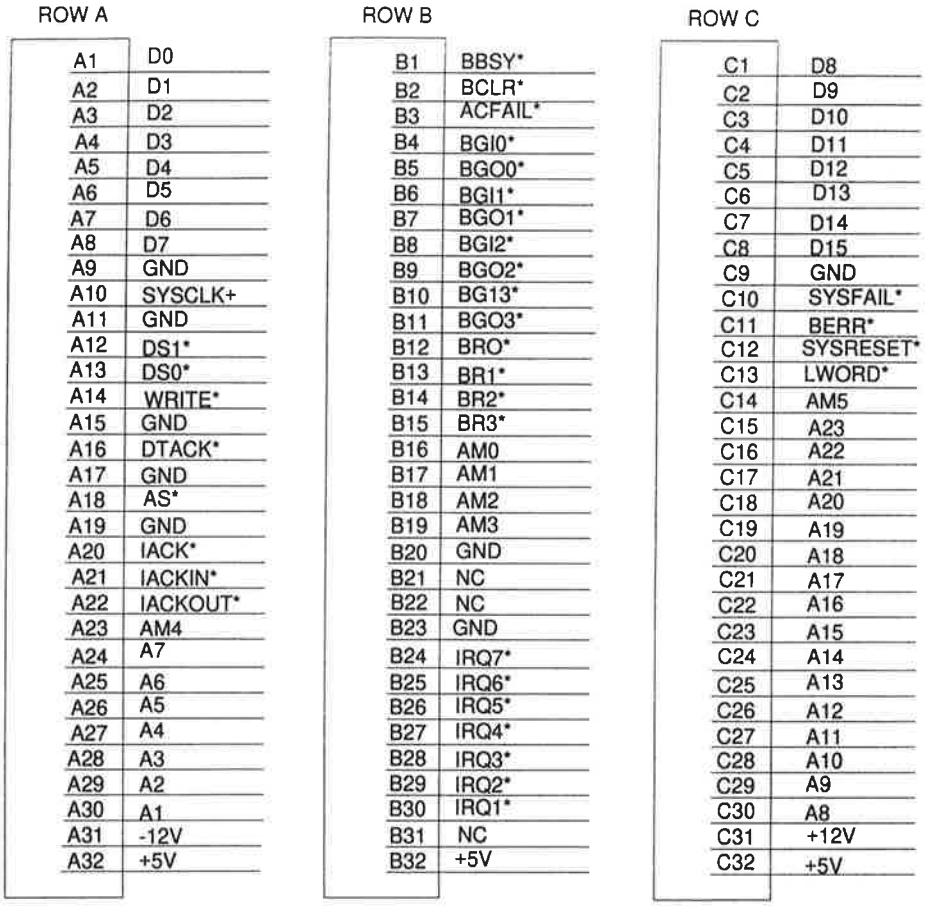
Table 7-11. **VMEbus P2 Connector Pinout of User-defined Signals** (Continued)

Pin	Signal Name	Description	Direction
C9	+5V	+5V	
C10	NC	Not Connected	
C11	GND	GND	
C12	GND	GND	
C13	AUX_SCSI _D0	SCSI #2 Data 0	Input / Output
C14	AUX_SCSI _D1	SCSI #2 Data 2	Input / Output
C15	AUX_SCSI _D3	SCSI #2 Data 3	Input / Output
C16	AUX_SCSI _D4	SCSI #2 Data 4	Input / Output
C17	AUX_SCSI _D5	SCSI #2 Data 5	Input / Output
C18	AUX_SCSI _D6	SCSI #2 Data 6	Input / Output
C19	AUX_SCSI _D7	SCSI #2 Data 7	Input / Output
C20	AUX_SCSI _D8	SCSI #2 Data 8	Input / Output
C21	AUX_SCSI _PAR0	SCSI #2 Parity	Input / Output
C22	GND	GND	
C23	AUX_SCSI _CD_L	SCSI #2 Control / Data	Output
C24	AUX_SCSI_REQ_L	SCSI #2 Request	Output
C25	AUX_SCSI_IO_L	SCSI #2 Input / Output	Output
C26	AUX_SCSI_SEL_L	SCSI #2 Select	Output
C27	+5V	+5V	Output
C28	+3.3V	+3.3V	
C29	+3.3V	+3.3V	
C30	+3.3V	+3.3V	
C31	GND	GND	
C32	+5V	+5V	Output

7.4 I/O Board Connectors

Described below are the connectors located on the I/O Board of the USP-1. Included are illustrations and/or tables featuring a complete listing of the connector pinouts.

7.4.1 VMEbus P1 Connector (I/O Board)



ROW A		ROW B		ROW C	
A1	D0	B1	BBSY*	C1	D8
A2	D1	B2	BCLR*	C2	D9
A3	D2	B3	ACFAIL*	C3	D10
A4	D3	B4	BGI0*	C4	D11
A5	D4	B5	BGO0*	C5	D12
A6	D5	B6	BGI1*	C6	D13
A7	D6	B7	BGO1*	C7	D14
A8	D7	B8	BGI2*	C8	D15
A9	GND	B9	BGO2*	C9	GND
A10	SYSCLK+	B10	BG13*	C10	SYSFAIL*
A11	GND	B11	BGO3*	C11	BERR*
A12	DS1*	B12	BRO*	C12	SYSRESET*
A13	DS0*	B13	BR1*	C13	LWORD*
A14	WRITE*	B14	BR2*	C14	AM5
A15	GND	B15	BR3*	C15	A23
A16	DTACK*	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	AS*	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	IACK*	B20	GND	C20	A18
A21	IACKIN*	B21	NC	C21	A17
A22	IACKOUT*	B22	NC	C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	IRQ7*	C24	A14
A25	A6	B25	IRQ6*	C25	A13
A26	A5	B26	IRQ5*	C26	A12
A27	A4	B27	IRQ4*	C27	A11
A28	A3	B28	IRQ3*	C28	A10
A29	A2	B29	IRQ2*	C29	A9
A30	A1	B30	IRQ1*	C30	A8
A31	-12V	B31	NC	C31	+12V
A32	+5V	B32	+5V	C32	+5V

Figure 7-9. **I/O Board VMEbus P1 Connector Pinouts**

Table 7-12. **VMEbus P1 Signal Descriptions -- I/O Board**

Pin	Signal Name	Description
A1	D0	Data 0
A2	D1	Data 1
A3	D2	Data 2
A4	D3	Data 3
A5	D4	Data 4
A6	D5	Data 5

Table 7-12. **VMEbus P1 Signal Descriptions -- I/O Board**

Pin	Signal Name	Description
A7	D6	Data 6
A8	D7	Data 7
A9	GND	Ground
A10	SYSCLK+	System Clock
A11	GND	Ground
A12	DS1*	Data Strobe 1
A13	DS0*	Data Strobe 0
A14	WRITE*	Read/Write
A15	GND	Ground
A16	DTAC*	Data Transfer Acknowledge
A17	GND	Ground
A18	AS*	Address Strobe
A19	GND	
A20	IACK*	Interrupt Acknowledge
A21	IACKI*	Interrupt Acknoledge
A22	IACKO*	Address Modilfier 4
A23	AM4	
A24	A7	Address 7
A25	A6	Address 6
A26	A5	Address 5
A27	A4	Address 4
A28	A3	Address 3
A29	A2	Address 2
A30	A1	Address 1
A31	-12 V	
A32	+5V	
C1	D8	Data Strobe 8
C2	D9	Data Strobe 7
C3	D10	Data Strobe 6
C4	D11	Data Strobe 5
C5	D12	Data Strobe 4
C6	D13	Data Strobe 3
C7	D14	Data Strobe 2
C8	D15	Data Strobe 1
C9	GND	Ground

Table 7-12. **VMEbus P1 Signal Descriptions -- I/O Board**

Pin	Signal Name	Description
C10	SYSFAIL*	System Fail
C11	BERR*	Bus Error
C12	SYSRESET*	System Reset
C13	LWORD*	Longword
C14	AM5	Address Modifier 5
C15	A23	Address 23
C16	A22	Address 22
C17	A21	Address 21
C18	A20	Address 20
C19	A19	Address 19
C20	A18	Address 18
C21	A17	Address 17
C22	A16	Address 16
C23	A15	Address 15
C24	A14	Address 14
C25	A13	Address 13
C26	A12	Address 12
C27	A11	Address 11
C28	A10	Address 10
C29	A9	Address 9
C30	A8	Address 8
C31	+12 V	
C32	+5 V	

7.4.2 VMEbus P2 Connector (I/O Board)

ROW A		ROW B		ROW C	
A1	AUI_12V	B1	+5V	C1	NC
A2	GND	B2	GND	C2	GND
A3	AUI_CIN	B3	RETRY*	C3	AUI_DIN
A4	AUI_CIP	B4	A24	C4	AUI_DIP
A5	PAR_IN_L_CONN	B5	A25	C5	AUI_DON
A6	PAR_DS_L_CONN	B6	A26	C6	AUI_DOP
A7	PAR_ACK_L_CONN	B7	A27	C7	FD_DEN_SEL
A8	PAR_BUSY_L_CONN	B8	A28	C8	FD_INDEX
A9	PAR_PE_CONN	B9	A29	C9	FD_MOT_EN
A10	PAR_SELECT_CONN	B10	A30	C10	FD_DRV_SEL
A11	PAR_AFXN_L_CONN	B11	A31	C11	FD_DIR_SEL
A12	PAR_ERROR_L_CONN	B12	GND	C12	FD_STEP
A13	PAR_RESET_L_CONN	B13	+5V	C13	FD_WR_DAT
A14	PPD0	B14	D16	C14	FD_WR_GATE
A15	PPD1	B15	D17	C15	FD_TRK0
A16	PPD2	B16	D18	C16	FD_WR_PROT
A17	PPD3	B17	D19	C17	FD_RD_DAT
A18	PPD4	B18	D20	C18	FD_HD_SEL
A19	PPD5	B19	D21	C19	FD_DENSE
A20	PPD6	B20	D22	C20	FD_EJECT
A21	PPD7	B21	D23	C21	FD_DSKCHNG
A22	SCSI_DAT_0	B22	GND	C22	SCSI_ATN*
A23	SCSI_DAT_1	B23	D24	C23	SCSI_BSX*
A24	SCSI_DAT_2	B24	D25	C24	SCSI_ACK*
A25	SCSI_DAT_3	B25	D26	C25	SCSI_RESET*
A26	SCSI_DAT_4	B26	D27	C26	SCSI_MSG*
A27	SCSI_DAT_5	B27	D28	C27	SCSI_SEL*
A28	SCSI_DAT_6	B28	D29	C28	SCSI_CD*
A29	SCSI_DAT_7	B29	D30	C29	SCSI_REQ*
A30	SCSI_PAR0_L	B30	D31	C30	SCSI_IO*
A31	GND	B31	GND	C31	GND
A32	REAR_SCSI_L	B32	+5V	C32	TERMPOWER

Figure 7-10. **VMEbus P2 Connector Pinouts (I/O Board)**

The VMEbus P2 Connector accommodates user-defined signals. The optional paddleboard is one way of easily accessing the USP-1 VMEbus P2 Connector user-defined signals. The following table lists the VMEbus P2 Connector user-defined signals.

Table 7-13. **VMEbus P2 Connector Pinout of User-defined Signals**

Pin	Signal Name	Description	Direction
A1	AUI_12V	AUI #1 +12V	
A2	GND	Ground	
A3	AUI_CIN	AUI #1Collision (-)	Input
A4	AUI_CIP	AUI #1 Collision (+)	Input
A5	PAR_IN_L	Parallel Port Select In	Output
A6	PAR_DS_L	Parallel Port Data Strobe	Input / Ouput
A7	PAR_ACK_L	Parallel Port Acknowledge	Input / Output
A8	PAR_BUSY_L	Parallel Port Busy	Input / Output
A9	PAR_PE	Parallel Port Paper Error	Input / Output
A10	PAR_SELECT	Parallel Port Select	Input / Ouput
A11	PAR_AFXN_L	Parallel Port Auto Feed	Output
A12	PAR_ERROR_L	Parallel Port Initialize	Output
A13	PAR_RESET_L	Parallel Port Error	Input / Output
A14	PPD0	Parallel Port Data 0	Input / Output
A15	PPD1	Parallel Port Data 0	Input / Output
A16	PPD2	Parallel Port Data 0	Input / Output
A17	PPD3	Parallel Port Data 0	Input / Output
A18	PPD4	Parallel Port Data 0	Input / Output
A19	PPD5	Parallel Port Data 0	Input / Output
A20	PPD6	Parallel Port Data 0	Input / Output
A21	PPD7	Parallel Port Data 0	Input / Output
A22	SCSI_DAT0	SCSI #1 Data 0	Input / Output
A23	SCSI_DAT1	SCSI #1 Data 1	Input / Output
A24	SCSI_DAT2	SCSI #1 Data 2	Input / Output
A25	SCSI_DAT3	SCSI #1 Data 3	Input / Output
A26	SCSI_DAT4	SCSI #1 Data 4	Input / Output
A27	SCSI_DAT5	SCSI #1 Data 5	Input / Output
A28	SCSI_DAT6	SCSI #1 Data 6	Input / Output
A29	SCSI_DAT7	SCSI #1 Data 7	Input / Output
A30	SCSI_PAR0_L	SCSI #1 Parity	Input / Output
A31	GND	GND	
A32	REAR_SCSI_L	SCSI #1 Auto Sense	Input

Table 7-13. **VMEbus P2 Connector Pinout of User-defined Signals** (Continued)

Pin	Signal Name	Description	Direction
C1	NC	No Connection	
C2	GND	Ground	
C3	AUI_DIN	AUI #1 Receive Data (-)	Input
C4	AUI_DOP	AUI #1 Receive Data (+)	Input
C5	AUI_DON	AUI #1Transmit Data (-)	Output
C6	AUI_DOP	AUI #1Transmit Data (+)	Output
C7	FD_DEN_SEL	Floppy Density Select	Output
C8	FD_INDEX	Track Index	Input
C9	FD_MOT_EN	Floppy Motor Enable	Output
C10	FD_DRV_SEL	Floppy Drive Select	Output
C11	FD_DIR	Head Step Direction	Output
C12	FD_STEP	Drive Step Pulse	Output
C13	FD_WR_DAT	Write Data	Output
C14	FD_WR_GATE	Write Enable	Output
C15	FD_TRK0	Track and Indicator	Input
C16	FD_WR_PROT	Write Protect	Input
C17	FD_RD_DAT	Read Data	Input
C18	FD_HD_SEL	Head Select	Output
C19	FD_DENSE	Density Select	Output
C20	FD_EJECT	Floppy Eject	Output
C21	FD_DSKCHNG	Disk Change	Input
C22	SCSI_ATN*	SCSI #1 Attention	Input / Output
C23	SCSI_BSY*	SCSI #1 Busy	Input / Output
C24	SCSI_ACK*	SCSI #1 Acknowledge	Input / Output
C25	SCSI_RESET*	SCSI #1 Reset	Input / Output
C26	SCSI_MSG*	SCSI #1 Message	Input / Output
C27	SCSI_SEL*	SCSI #1 Select	Input / Output
C28	SCSI_CD*	SCSI #1 Command / Data	Input / Output
C29	SCSI_REQ*	SCSI #1 Request	Input / Output
C30	SCSI_IO*	SCSI #1 Input / Output	Input / Output
C31	GND	Ground	
C32	TERMPOWER	SCSI #1 Termination Power	

7.5 SBus Connectors #1 and #2

GND	1	49	CLK0/1
BR0/1*	2	50	BG0/1
SEL0/1*	3	51	AS*
SINT1	4	52	GND
D0	5	53	D1
D2	6	54	D3
D4	7	55	D5
INT2	8	56	+5V
D6	9	57	D7
D8	10	58	D9
D10	11	59	D11
INT3	12	60	GND
D12	13	61	D13
D14	14	62	D15
D16	15	63	D17
INT4	16	64	+5V
D19	17	65	D18
D21	18	66	D20
D23	19	67	D22
INT5	20	68	GND
D25	21	69	D24
D27	22	70	D26
D29	23	71	D28
INT6	24	72	+5V
D31	25	73	D30
SIZ0	26	74	SIZ1
SIZ2	27	75	RD
INT7	28	76	GND
PA0	29	77	A1
PA2	30	78	A3
PA4	31	79	A5
LERR*	32	80	+5V
PA6	33	81	A7
PA8	34	82	A9
PA10	35	83	A11
ACK0*	36	84	GND
A12	37	85	A13
A14	38	86	A15
A16*	39	87	A17
ACK1	40	88	+5V
A18	41	89	A19
A20	42	90	A21
A22	43	91	A23
ACK2*	44	92	GND
A24	45	93	A25
A26	46	94	A27
DP	47	95	RST*
-12V	48	96	+12V

Figure 7-11. **SBus Connectors #1 and #2 Pinouts**

7.6 Paddleboard Connectors

The paddleboard is designed for connecting external devices (SCSI devices, serial devices, parallel devices, floppy drives, and AUI ethernet) to the USP-1. Described below are the connectros located on the optional USP-1 Paddleboard. Included are illustrations and/or tables featuring a complete listing of the connector pinouts. This is applicable to both SCSI #1 and SCSI #2 access off the paddle bord.

GND	1	26	SCSI_D0
GND	2	27	SCSI_D1
GND	3	28	SCSI_D2
GND	4	29	SCSI_D3
GND	5	30	SCSI_D4
GND	6	31	SCSI_D5
GND	7	32	SCSI_D6
GND	8	33	SCSI_D7
GND	9	34	SCSI_PAR0
GND	10	35	GND
GND	11	36	REAR_SCSI*
GND	12	37	GND
NC	13	38	TERMPOWER
GND	14	39	GND
GND	15	40	GND
GND	16	41	SCSI_ATN*
GND	17	42	GND
GND	18	43	SCSI_BSY*
GND	19	44	SCSI_ACK*
GND	20	45	SCSI_RST*
GND	21	46	SCSI_MSG*
GND	22	47	SCSI_SEL*
GND	23	48	SCSI_CD*
GND	24	49	SCSI_REQ*
GND	25	50	SCSI_IO*

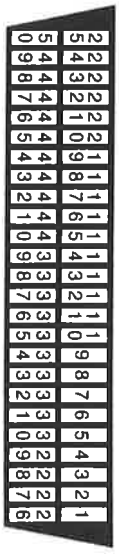


Figure 7-12. **SCSI Paddleboard Connector Pinouts**

Table 7-14. **SCSI Paddleboard Connector Pinouts**

Pin	Signal Name	Description	Direction
1	GND	Ground	
2	GND	Ground	
3	GND	Ground	
4	GND	Ground	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	NC	Not Connected	

Table 7-14. **SCSI Paddleboard Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction
14	GND	Ground	
15	GND	Ground	
16	GND	Ground	
17	GND	Ground	
18	GND	Ground	
19	GND	Ground	
20	GND	Ground	
21	GND	Ground	
22	GND	Ground	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	SCSI_D0	Data Bit	Input / Output
27	SCSI_D1	Data Bit	Input / Output
28	SCSI_D2	Data Bit	Input / Output
29	SCSI_D3	Data Bit	Input / Output
30	SCSI_D4	Data Bit	Input / Output
31	SCSI_D5	Data Bit	Input / Output
32	SCSI_D6	Data Bit	Input / Output
33	SCSI_D7	Data Bit	Input / Output
34	SCSI_PAR0	Parity	Input / Output
35	GND	Ground	
36	REAR_SCSI*	SCSI Auto Sense - Paddle-board	Input
37	GND	Ground	
38	TERMPOWER	Termination Power	
39	GND	Ground	
40	GND	Ground	
41	SCSI_ATN*	Attention	Output
42	GND	Ground	
43	SCSI_BSY*	Busy	Input / Output
44	SCSI_ACK*	Acknowledge	Output
45	SCSI_RST*	Reset	Input / Output
46	SCSI_MSG*	Message	Input
47	SCSI_SEL*	Select Output	Input / Output

Table 7-14. **SCSI Paddleboard Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction
48	SCSI_CD*	Control / Data	Input
49	SCSI_REQ*	Request Output	Input / Output
50	SCSI_IO*	Input / Output Control	Output

7.6.1 TTY Connectors

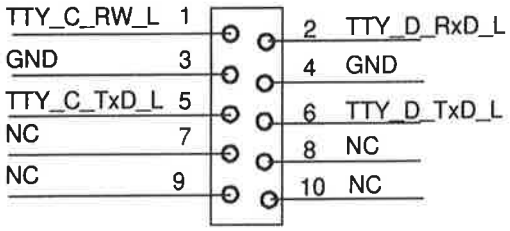


Table 7-15. **TTY C/D Connector**

PIN	Signal	Description	Direction
1	TTY_C_RxD_L	Receive Data C	In
2	TTY_D_RxD_L	Receive Data D	In
3	GND	Ground	
4	TTY_C_TxD_L	Transmit Data C	Out
5	TTY_D_Txd_L	Transmit Data D	Out
6	NC	Not Connected	
7	NC	Not Connected	
8	NC	Not Connected	
9	NC	Not Connected	
10	NC	Not Connected	

7.6.2 Parallel Port Connector

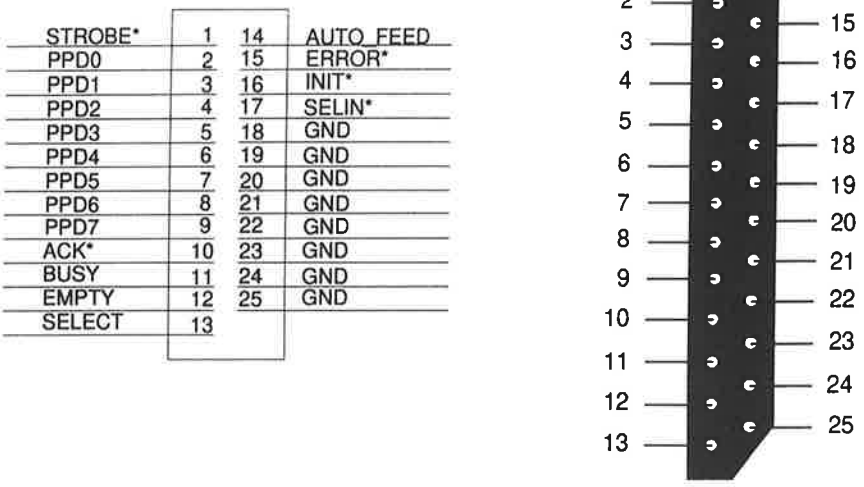


Figure 7-13. **Parallel Port Connector Pinouts**

Table 7-16. **Parallel Port Connector Pinouts**

Pin	Signal Name	Description	Direction
1	STROBE*	Data Strobe	Input / Output
2	PPD0	Data Bit	Input / Output
3	PPD1	Data Bit	Input / Output
4	PPD2	Data Bit	Input / Output
5	PPD3	Data Bit	Input / Output
6	PPD4	Data Bit	Input / Output
7	PPD5	Data Bit	Input / Output
8	PPD6	Data Bit	Input / Output
9	PPD7	Data Bit	Input / Output
10	ACK*	Acknowledge	Input / Output
11	BUSY	Busy	Input / Output
12	EMPTY	Paper Empty	Input
13	SELECT	Select	Input
14	AUTO_FEED	Auto Feed	Output
15	ERROR*	Error	Input
16	INIT*	Reset	Output
17	SELIN*	Select In	Output
18	GND	Ground	
19	GND	Ground	

Table 7-16. **Parallel Port Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction
20	GND	Ground	
21	GND	Ground	
22	GND	Ground	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	

7.6.3 Ethernet AUI Connectors

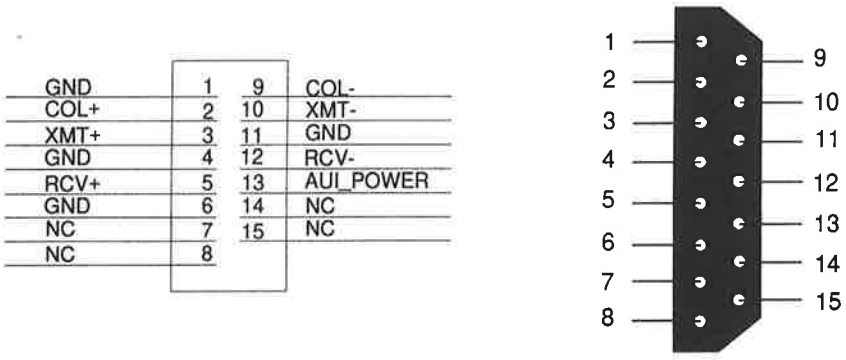


Figure 7-14. **Ethernet AUI Connector Pinouts**

Table 7-17. **Ethernet AUI Connector Pinouts**

Pin	Signal Name	Description	Direction
1	GND	Ground	
2	COL+	Collision (+)	Input
3	XMT+	Transmit Data (+)	Output
4	GND	Ground	
5	RCV+	Receive Data (+)	Input
6	GND	Ground	
7	NC	Not Connected	
8	NC	Not Connected	
9	COL-	Collision (-)	Input
10	XMT-	Transmit Data (-)	Output
11	GND	Ground	
12	RCV-	Receive Data (-)	Input
13	AUI_POWER	+12V	Output

Table 7-17. **Ethernet AUI Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction
14	NC	Not Connected	
15	NC	Not Connected	

7.6.4 Floppy Port Connector

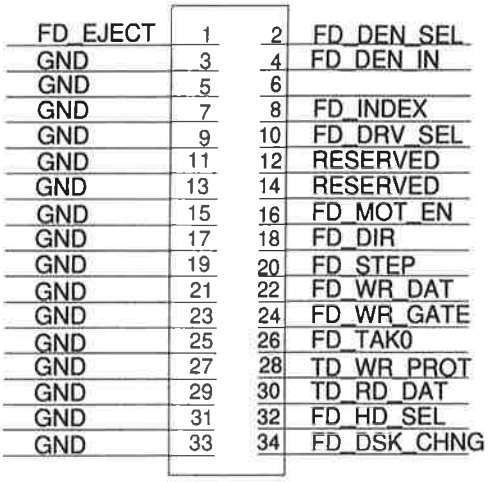


Figure 7-15. **Floppy Port Connector Pinouts**

Table 7-18. **Floppy Port Connector Pinouts**

Pin	Signal Name	Description
1	FD_EJECT	Floppy Eject
2	FD_DEN_SEL	Density Eject
3	GND	Ground
4	FD_DEN_IN	Density Sense Input
5	GND	Ground
6	NC	Not Connected
7	GND	Ground
8	FD_INDEX	Track Index
9	GND	Ground
10	FD_DRV_SEL	Floppy Drive Select
11	GND	Ground
12	RESERVED	
13	GND	Ground
14	RESERVED	
15	GND	Ground

Table 7-18. **Floppy Port Connector Pinouts**

Pin	Signal Name	Description
16	FD_MOT_EN	Floppy Moter Enable
17	GND	Ground
18	FD_DIR	Head Step Direction
19	GND	Ground
20	FD_STEP	Drive Step Pulse
21	GND	Ground
22	FD_WR_DAT	Write Data
23	GND	Ground
24	FD_WR_GATE	Write Enable
25	GND	Ground
26	FD_TAK0	Track 0 Indicator
27	GND	Ground
28	FD_WR_PROT	Write Protect
29	GND	Ground
30	FD_RD_DAT	Read Data
31	GND	Ground
32	FD_HD_SEL	Head Select
33	GND	Ground
34	FD_DSK_CHNG	Disk Change

8.1 Overview

The system achieves a high level of integration through ASICS. The ASICs include Uniprocessor System Controller (USC), UPA to SBus Interface (U2S), Reset/Interrupt/Clock Controller (RIC), and the Cross Bar Switch (XBI). All ASICs are 1149.1 JTAG compliant. Refer to Table 8-1 for some characteristics.

Table 8-1. **Summary of System ASIC Characteristics**

Chip Name	Gates	RAM (bits)	Tech	Package	Die Size (mmxmm)	Power	Chips/ system
USC	65K	0	0.5.	5BGA	7.2.7.2	2.2W	1
XBI (BiCMOS)	7K	0	0.6.	48TSSOP		0.2W	18
RIC	7k	0	0.9.	160MQFP	6.25x6.25	0.4W	1
U2S	116K	14K	0.5.	372BGA	10.10	2.7W	1
MACIO #1	60K	(inc)	0.7.	160PQFP	11.07.11.7 6	1.4W	1
MACIO #2	60K	(inc)	0.7.	160PQFP	11.07.11.7 6	1.4W	1
SLAVIO	40K	0	0.7.	160PQFP	9.44x9.16	0.28W	1
APC	13K	0	1.0.	120PQFP		0.37W	1

The USC controls the UPA and main memory, implementing accesses from UPA master device to UPA slave device and UPA to memory. Some feature of the USC are:

- Integrates memory controller functionality
- Supports four banks of memory, each with 1 Memory Module
- Supports Memory Modules with 4 MByte, 16 MByte, and 64 MByte 50/60 ns DRAM
- Maximum memory configurations of 1 GByte
- Supports 2 UPA masters and one UPA slave with independent address busses (independent busses are required for graphics streaming)
- Controls the XBI, which connects the UPA Data bus and memory
- up to 100 MHz operation

- 225 pin BGA package
- 3.3V and 5V power supply voltage.

8.2 UPA to SBus Interface (System I/O Controller) (U2S)

The U2S bridges between the UPA and the SBus. Feature of this interface are:

- Contains the IOMMU
- Integrated streaming cache to enhance sequential 10 performance
- Logic for dispatching interrupt vectors to processors
- ECC generation and checking logic
- 372 pin BGA package
- 3.3V and 5V supply voltages.

8.3 Cross Bar Switch (XB1)

The XB1 chip is a three port crossbar connecting a 144 bit UPA data bus, a 288 bit wide DRAM memory bus, and a 72 bit UPA data bus. To maintain a manageable pin count, the devices are sliced so that 18 parts are needed to form the complete switch function. Some features of the XB1 are:

- 8 bits of UPA128, 4 bits of UPA72, and 16 bits of DRAM bus per chip
- 100 MHz maximum clock rate
- 3.3V and 5V power supply voltage
- Switch connections controlled by USC
- 48 pin TSSOP package.

8.4 Reset, Interrupt, Scan and Clock controller (FJC)

The FJC chip implements 4 functions: reset, interrupts, scan, and clock. Generation and stretching of the reset pulse is performed in this ASIC. Interrupt logic concentrates 42 different interrupt sources into a 6 bit code that communicates with the U2S chip. It also integrates a JTAG Controller. In cases where there are multiple processors, they are required to run at the same frequency. A 3 bit code is output by each module to indicate the speed for that module. Logic inside RIC determines what the minimum value of the codes presented to it is, and outputs this for the rest of the clock logic to set the main system frequency. In summary, the features of the RIC include:

- Determination of system clock frequency
- Control of reset generation
- JTAG
- Execution of SBus and miscellaneous interrupt concentration for U2S

- Control of Flash PROM programming, frequency margining, and lab console operation
- 25 MHz operation
- 160 pin MQFP package
- 5V operation.

8.5 MACIO #1

MACIO #1 implements FAST-narrow SCSI, 10Base_T, Ethernet, and parallel port connections. Features include:

- Integrates 10 MByte/sec SCSI interface core
- Integrates 10 MByte/sec ethernet
- Complies with IEEE 1496 SBus specification
- 25 MHz SBus operation
- 5V supply voltage.

8.6 MACIO #2

The MACIO #2 implements FAST-narrow SCSI and AUI ports. MACIO #2 meets the same, relevant specifications as the MACIO #1.

8.7 SLAVIO

SLAVIO integrates Serial Ports and EBus control. The features of the SLAVIO include:

- Sunness I/O devices to Ebus interface
- Floppy interface (82077) supporting transfers up to 1 MByte/second
- Integrated keyboard/mouse interface - 2 Serial Port Controllers (asynchronous only) (85C30)
- Provides 2 Synchronous / Asynchronous Serial Port Controllers (85C30)
- Interrupt, Reset, Counter / Timer functions
- Auxiliary I/O for LED, power-management, and floppy control
- Complies with IEEE 1496 SBus specification
- 25MHz SBus operation
- 5V supply voltage.

8.8 Aurora Personality Chip (APC)

The APC ASIC is utilized to provide audio functionality. Following is the list of features used on the System:

- Connects to Crystal Semiconductor Codec CS4231 (or compatible devices)
- Audio DMA controller
- Power management
- Complies with IEEE 1496 SBus specification
- 120PQFP
- 5V supply voltage.

9

Reset

9.1 Overview

This chapter covers system generated resets. Other types of resets, generated and observed only by the local processor, are not described in this chapter. Examples of resets not covered in this chapter are Software-Initiated Reset (SIR) and Watchdog Reset (WDR).

Resets are used to force all or part of the system into a known state. In the USP-1, resets are sourced from power supply, push-button, scan interface, software, error conditions, and power management logic. They are converted into three types of resets in the system, power-on-reset (POR), externally initiated reset (XIR), and UPA arbiter reset. Their assertions have different level of effects on the system. Information stored in the USC Control Register allows software to determine where the reset originated.

9.2 Reset Sources

Resets come form various sources. They are converted by the System Controller into two sets of signals, UPA_RESET_L <1:0> and UPA_XIR_L. Processor(s) receiving UPA_RESET_L <0> will treat the assertion of this signal as a POR. The U2S receives both UPA_RESET_L <1:0> reset signals. The UPA_RESET_L <0> signal is used by the U2S as an UPA Arbiter Reset. UPA graphic devices receive an UPA_RESET_L<1>. Separate UPA_RESET_L signals are needed for the processor and U2S / Graphics for power management reasons. The U2S will use the UPA_RESET_L<1> signal to derive an SBUS_RESET_ for on-board I/O devices and SBus slots. The XIR reset is only observed by the processor. The System Controller will assert UPA_XIR_L for one clock cycle when it detects an XIR condition. The following block diagram in *Figure 9-1* shows how resets are generated and distributed in the system.

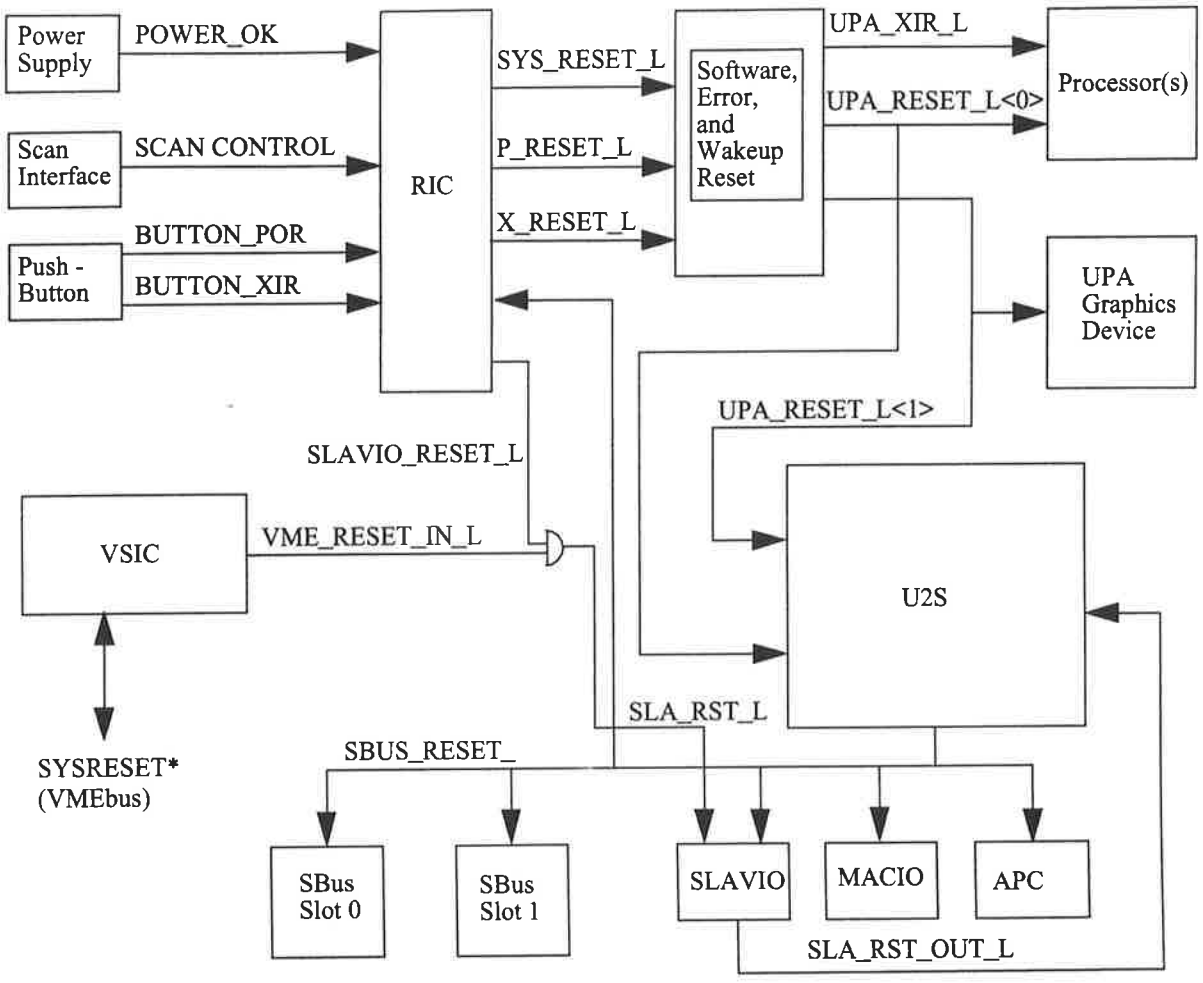


Figure 9-1. **Reset Block Diagram**

The assertion of UPA-RESET_L<1:0> is asynchronous with the UPA clock while UPA_XIR_L is synchronous with the UPA clock. The deassertion edge of the resets has to be synchronous with UPA clock. The assertion of SBUS_RESET_ can be asynchronous with SBus clock. The deassertion edge of SBUS_RESET_ must be synchronous with SBus clock.

9.2.1 Hardware Reset Sources

The five different resets that RIC detects are: Power Supply POR, Push-button POR, Push-button XIR, Scan POR, and Scan XIR. The RIC chip combines the five reset conditions into three signals to the System Controller. Based on these signals from the RIC, the System Controller will set the proper bit(s) in the USC Control Register to allow software to identify the reset source.

9.2.1.1 Power Supply POR

After the system power supply is turned on and before the power supply output stabilizes, the power supply will drive the POWER_OK signal inactive to put the system in a reset state. When the supply voltage reaches a level to support a functional system, the power supply will drive the POWER_OK active. The RIC chip uses this signal to generate power-on-reset (POR) during the period POWER_OK is inactive to reset the entire system. It extends the reset period for 12.8 ms after the POWER_OK signal becomes active. The extra time is needed to allow the PLL circuitry to stabilize. The RIC chip asserts SYS_RESET_L to the System Controller during the whole reset period. Since the SBus clock is also derived from the synthesizer which has PLL circuitry in it, the RIC chip cannot use it as the source for the internal counter. The RIC chip will use a 10 MHz clock to count the extended reset time.

9.2.1.2 Push-button POR

An external push-button is provided to allow the user to trigger a reset to the system. Two types of push-button resets are available, Push-button POR and Push-button XIR. A Push-button POR has the same effect as a Power Supply POR. The only difference between these two is the status bits in USC Control Register and the state of refresh (unchanged with B_POR). The P_BUTTON bit will be set to indicate the reset is initiated by a push-button POR.

9.2.1.3 Push-button XIR

A push-button XIR is provided to allow the user to reset part of the processor without resetting the whole system. The System Controller will set the X_BUTTON bit in the USC Control Register when a Push-button XIR is detected. An XIR affects processors only. It has no effect on the rest of the system, such as the USC, the U2S, memory, and any I/O devices. The effect of an XIR on the UltraSPARC-1 processor is different from POR. Additional detailed information can be found in the USP-1 Programmer's Reference Manual.

9.2.1.4 Scan POR

The scan controller can also assert reset to the system through the scan interface. A Scan POR has the same effect as a POR from the power supply. It shares the same status bit as the Push-button POR. The System Controller does not see the difference between Scan POR and Push-button POR. The same status bit P_BUTTON will be set in the USC Control Register.

9.2.1.5 Scan XIR

The scan controller can scan in a command to the RIC to cause a Scan XIR. This has the same effect as a Push-button XIR. The Scan XIR and Push-button XIR share the same status information in the USC Control Register.

Note — Do not assert a Push-button POR or Push-button XIR while coming out of a system reset (power on condition). This activates a special test mode in the USC chip which results in a shortened reset.

9.2.1.6 SYSRESET*

If SYSRESET* is asserted by another VMEbus board and the USP-1 is jumpered to receive it, the U2S will assert an SBus reset (SB_RESET_L) to the system I/O devices.

9.2.2 Software Reset

9.2.2.1 Software POR

Software can also generate a POR equivalent reset by setting the SOFT_POR bit in the USC Control Register. This is different from SIR supported in UltraSPARC-1, which is only observed by the initiating processor. A Software POR has the same effect as POR except that the refresh is unchanged.

9.2.2.2 Software XIR

Software can also issue an XIR to the processors by setting the SOFT_MR bit in the USC Control Register. A Software XIR has the same effect as other XIRs. Once the bit is set it will remain set until software clears it. This allow software to find out what triggers previous XIR.

9.2.3 Error Reset

A fatal error in the system can also cause a system reset. A reset will be initiated if a fatal system error is detected. A fatal error reset has the same effect as other PORs. If the reset is caused by a fatal error, the FATAL bit in the USC Control Register will be set to indicate the reset source. The Themis USP-1 system detects the following fatal error conditions:

- UPA Address Parity Error detected by the USC
- Fatal Error conditions reported by UPA devices through a P_FERR UPA reply
- Master Request Queue Overflow in the USC.

9.2.4 Wake-up Reset

The UltraSPARC-1 processor and Themis USP-1 system provide power management support. One of the supported features is to allow the UltraSPARC-1 processor to enter a power-down mode by executing a shutdown instruction. A reset is the only method to wake up the processor after the UltraSPARC-1 / Cache / Tag / UDB are in power-down mode. The wake-up reset is generated by the USC when it detects an interrupt packet being directed to a port in power-down mode. This reset will only reset the processor(s) and UPA arbitration, not other system resources, such as memory, I/O devices. The UPA graphics interface will not be reset. The wake-up reset generated to the processor has the same effect as a POR. The WAKEUP status bit will be set in the USC Control Register to indicate the reset source.

9.2.5 UPA Arbitration Reset

The UPA uses distributed arbitration for master devices to gain control of the address bus. Each master device has its own arbiter to keep track of which master device owns the address bus and which master device should get the ownership of the bus if multiple requests are present.

A UPA_RESET_L <1:0> will reset the devices connected to it. During the wake-up sequence, a UPA_RESET_L <0> will be asserted to reset the processor and the U2S arbiter. A UPA_RESET_L <1> will not be asserted. This leaves the states of I/O devices and UPA Graphics unchanged.

9.3 Effects of Resets

All system resets are software visible and insure proper hardware operation. For example, all buses are tristated at power up.

9.3.1 Major System Activities as a Function of Reset

Table 9-1 shows the effects of the various different resets in an Themis USP-1 system.

Table 9-1. **System Reset Effects**

Reset Sources	USC Register[a]	Memory Refresh	Reset I/O Devices	Reset UPA Graphics	Reset UPA Arbiter	CPU XIR	UPA Reset to the CPU
Power Supply POR	Reset	Disable	Yes	Yes	Yes	No	Yes
Push-button POR	Reset	NC	Yes	Yes	Yes	No	Yes
Push-button XIR	NC	NC	No	No	No	Yes	No
Scan POR	Reset	NC	Yes	Yes	Yes	No	Yes
Scan XIR	NC	NC	No	No	No	Yes	No
Software POR	Reset	NC	Yes	Yes	Yes	No	Yes
Software XIR	NC	NC	No	No	No	Yes	No
Error Reset	Reset	NC	Yes	Yes	Yes	No	Yes
Wake-up Reset	NC	NC	No	No	Yes	No	Yes

a. NC = No Change. Bits in the USC Control Register will be set to the proper value based on the type of reset received by the USC.

9.3.2 Bus Conditions at Power up

It is important to insure that all buses are tristated at power up. This prevents drive fights. To be completely safe, these buses must tristate whether or not the device interfacing to them is being clocked. Otherwise, failure of a clock generator could cause permanent damage to a chip on the board. Bused system signals are:

- UPA Address Bus 0
- UPA Processor Data Bus
- UPA 64 bit Data Bus
- Memory Data Bus
- SBus
- EBus

9.3.2.1 UPA Address Bus 0

The two devices on this bus are the processor(s) and the U2S. The processor(s) and U2S tristate asynchronously upon detection of RESET.

9.3.2.2 UPA Processor Data Bus

This bus is shared by the UDBs and the BMX. The UDB chips tristate the data bus at reset. The BMX has a POR circuit which causes tristate its buses at power up time.

9.3.2.3 Memory Data Bus

This bus is driven by the DRAM and the BMX chip. The RAS* and CAS* signals driven by the USC are asynchronously deasserted. BMX tristates its data output pins at power up.

9.3.2.4 SBus

All expansion slots (U2S, MACIO, SLAVIO, and APC) share this bus. The U2S asynchronously tristates this bus. It also asynchronously de-asserts the AS line.

9.3.2.5 EBus

The PROM, TOD/NVRAM, and the USC share this bus. The RIC chip drives the PROM CS, and the USC chip select. All signals driven by the RIC asynchronously deassert. Unfortunately, SLAVIO does not asynchronously deassert its signals, so it is possible to have READ and the chip selects to the TOD and the PROM active if the SBus clock is not operational.

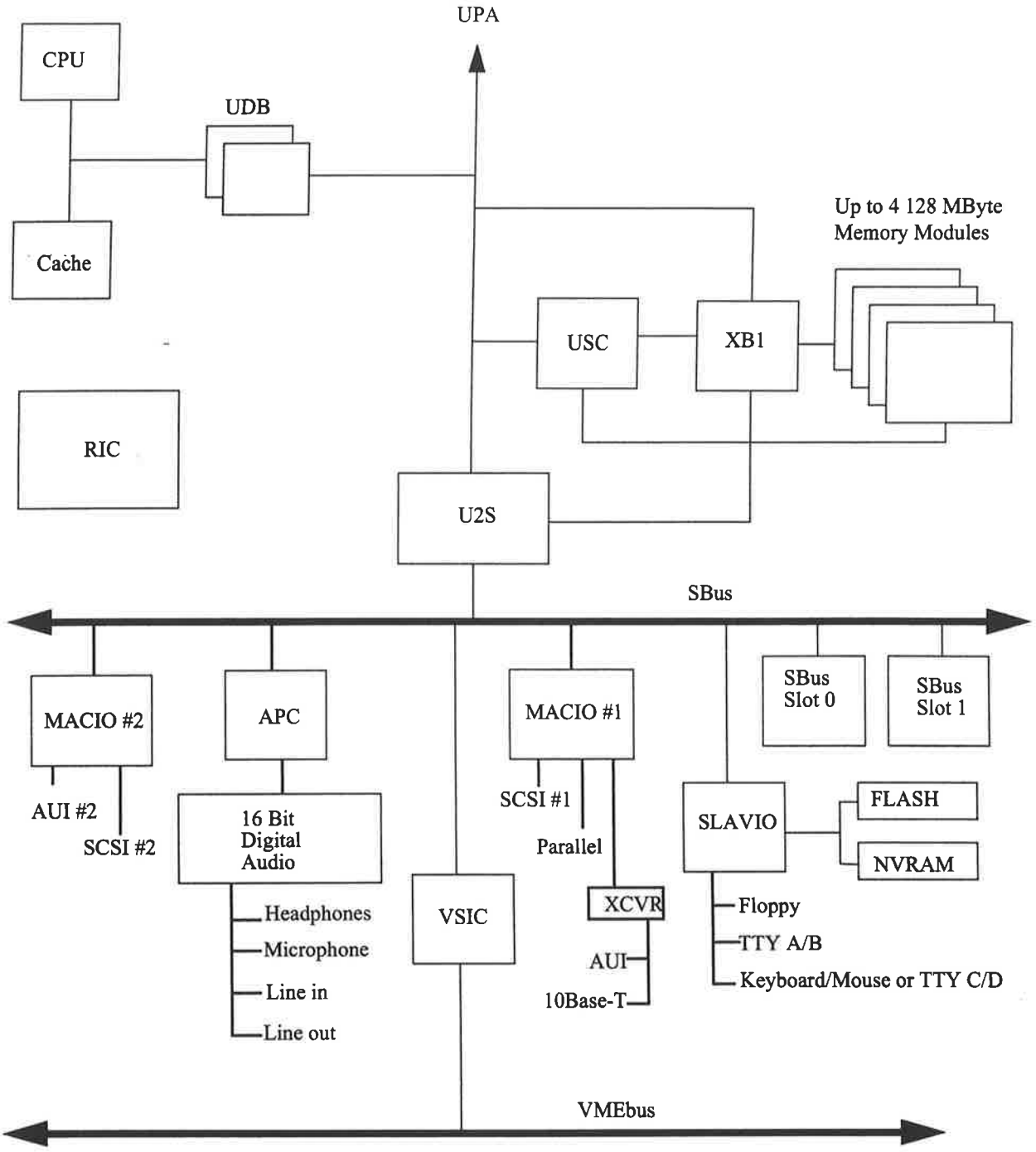


Figure 9-2. **Block Diagram of USP-1**

10.1 Overview

Clock generation for the major clocks is done through the use of frequency synthesizers. These components combine a voltage controlled oscillator (VCO) and a programmable divider to derive a high speed dock from a much lower speed crystal oscillator. A component has been selected which provides serial and parallel programming paths. See *Figure 10-1* for a simplified diagram of the component. In the USP-1 the parallel path is used for power up programming, and the serial path is used for frequency adjustment either to set the correct operating frequency, or for margining (under control of software).

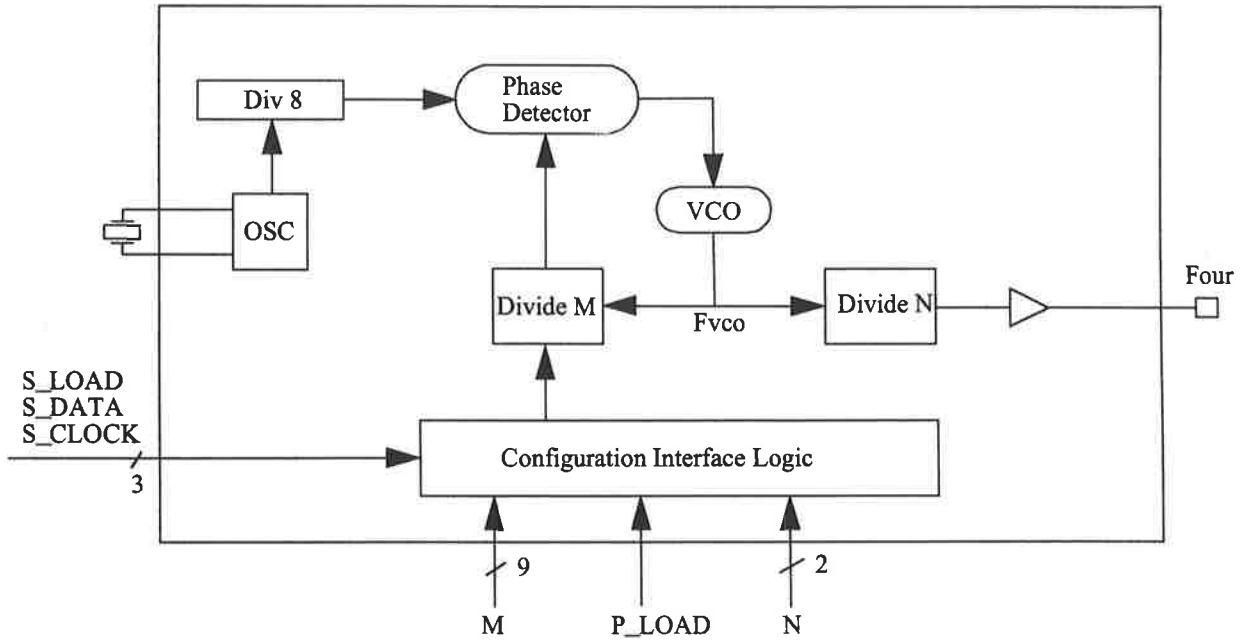


Figure 10-1. **Simplified Block Diagram of Clock Generator**

10.2 UPA and Processor Clocks

On the USP-1, the UPA and processor clocks are hard-wired. Refer to *Figure 10-2* for the logical architecture of the schematic. Specific components are not listed; other levels of buffering may be necessary.

A 3-bit code determines the frequency of operation. Circuitry within the RIC chip takes in four 3-bit codes and outputs the lowest. This will determine the frequency of operation of the CPU Clock. The 3-bit code is made visible through a register in the APC chip (the Fan Control Register: 0x1FF DA00 0020 - bits <3:1>). If software determines that the reset type is a POR, it should read this register, and use this value, preferably in conjunction with the CPU revision to index into a table which determines the desired operating frequency. By using lists of pointers to tables, where every list item corresponds to a different CPU revision, codes can be reused so long as CPU speeds are monotonically increasing for each revision. If the CPU revision is later than the last item in the list, then software could just use the last table. The code obtained from the lookup should be programmed into the UPA clock frequency generator and the system should be reset (using the serial load and reset address for the frequency margining registers).

The upper bit of the 3-bit code must be used to select the divide ratio. A value of '1' corresponds to a divide ratio of 3 while a value of '0' corresponds to a divide ratio of 2 between the UPA clock and the CPU clock. Since system PLLs require a minimum frequency in order to operate, bit 2 should also be used to set the default power up frequency for the processor. Recommended values are 128 MHz in divide by 2 and 164 MHz in divide by 3. These values will allow bit 2 to feed M[6] and M[4] of the clock generator in order to get the different frequencies.

Note — It is not possible to program only the CPU frequency. Software must also load the value for the SBus clock generator. However, its value is correct at power up, so software should load the default value of 100 MHz.

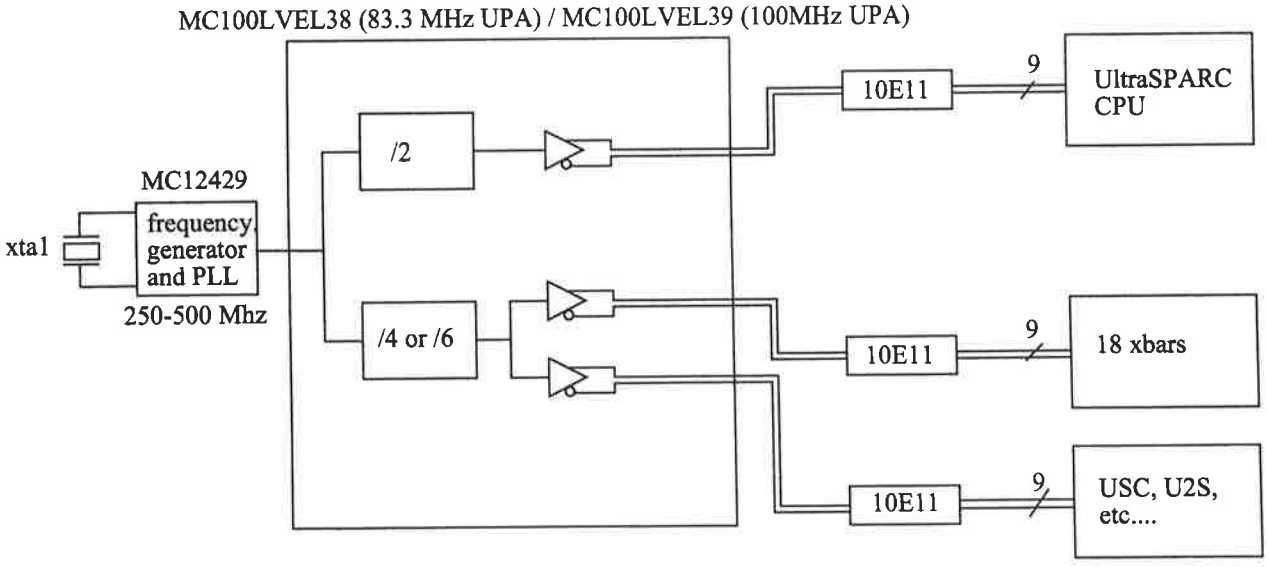


Figure 10-2. **SBus Reference Platform CPU and System Clock Schematic**

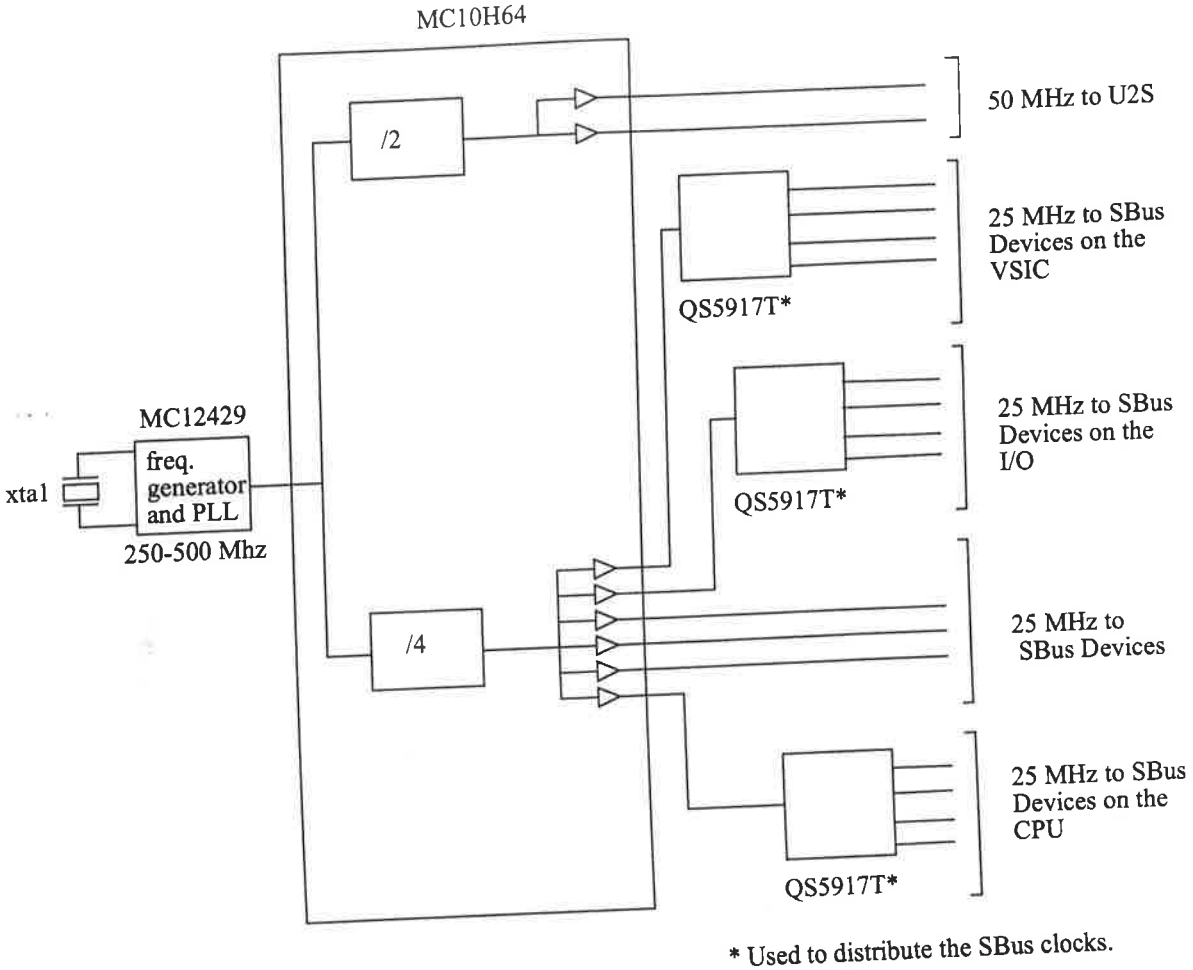


Figure 10-3. **SBus Ref. Platform SBUS Clock Schematic**

10.3 U2S and SBus Clocks

The U2S and the SBus clocks come from the same trunk and have a fixed 2:1 frequency ratio. While these clocks are software programmable, they default to 50 MHz and 25 MHz, respectively. Both clocks are on the TTL level.

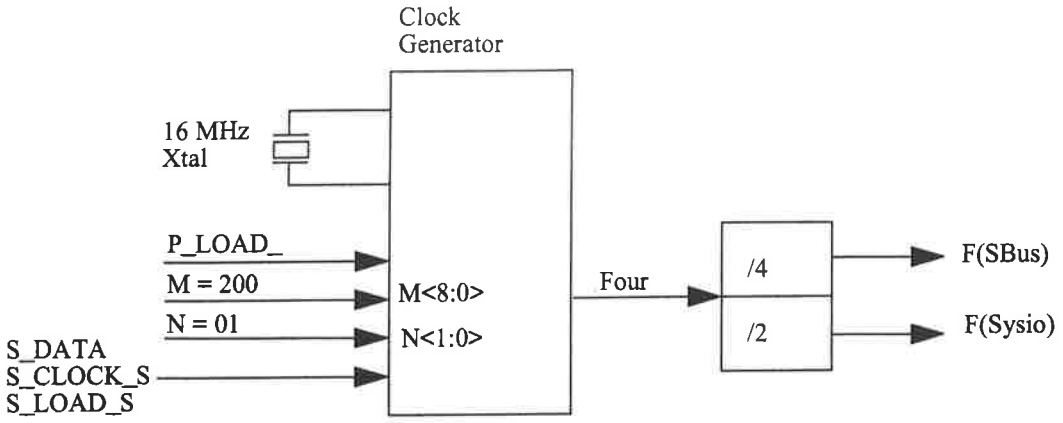


Figure 10-4. **SBus Clock**

10.4 Other Clocks

In addition to the clocks listed above, the following clocks or crystals are present in the system:

- 10 MHz - for Ethernet and U2S timers
- 24 MHz - for the Floppy Controller
- 40 MHz - for SCSI

10.5 Frequency Margining

Frequency margining involves changing the frequency of operation of the system away from the normal design point. Past systems have required physical replacement of an oscillator in order to change the frequency. Through the use of a programmable oscillator, this can be accomplished through software without changing the component.

Note — When margining the SBus clock, the software should be careful about the state of the MODE bit in the U2S Control Register. As the description of that bit states, it should be set to '0' if the UPA clock is running equal to or slower than the SBus clock.

10.6 Module Code versus Frequency

The table below shows the code for the various frequencies. The actual frequency achieved is the truncated value of the desired frequency.

Table 10-1. **Example Table of CPU and UPA Frequencies**

Code	Ideal TC_{CPU}	TC_{CPU} (ns)	F_{CPU} (MHz)	TC_{UPA} (ns)	F_{UPA} (MHz)	F_{CPU} / F_{UPA}	F_{OUT} (MHz)	M	N
0	7.5	7.52	133.0	15.04	66.50	2	266	266	1
1	7.0	6.99	143.0	13.99	71.50	2	286	286	1
2	6.5	6.49	154.0	12.98	77.00	2	308	308	1
3	6.0	6.01	166.5	12.02	83.25	2	333	333	1
4	5.5	5.51	181.5	16.53	60.50	3	363	363	1
5	5.0	5.00	200.0	15.00	66.70	3	400	400	1
6	4.5	4.50	222.0	13.51	74.00	3	444	444	1
7	4.0	4.00	250.0	12.00	83.30	3	500	500	1

11.1 Overview

An outline of system initialization, testing, and diagnostics are provided in this chapter. A table of FORTH Monitor based diagnostics is also provided.

11.2 Initialization

These steps must be performed before any access can be made to memory:

1. Determine the operating frequency of the system, then initialize the Mem_Cntl1 Register in the System Controller with the appropriate values for the given operating frequency.

2. DRAMs require a minimum of eight RAS cycles to initialize their internal circuitry before they can be accessed. These eight cycles are supplied by enabling refresh. Refresh is turned on by setting the RefEnable bit in the Mem_Cntl0 Register in the System Controller. RefInterval should be set to a value assuming a full memory system. Also, the MEMMODPresent bits should all be set to '1'.

After the probing step, RefInterval and MEMMODPresent can be set to the proper values. RefEnable must be off. A wait period must occur after RefEnable and before beginning the probe. The duration of the wait period is determined by:

- (8 Memory Modules) x (8 refreshes) x (RefInterval) x (8 clocks) x (clock period) seconds.

11.2.1 Memory Probing

The only way to determine the number of Memory Modules present in the system and what their sizes are is by probing. To probe a memory module perform writes to certain memory locations, read back the data, and examine the effects of the writes.

This section describes an algorithm for Memory Module probing that is based upon the behavior of the hardware and the Memory Module configurations supported. The algorithm takes advantage of the fact that writes to non-existent addresses can 'wrap around' and overwrite data in a valid location (assuming that a Memory Module is present). The algorithm below specifies what these addresses are. The memory block that is written to at each location should contain a unique signature, and should not consist of all 0's or all 1's.

All addresses for block write / read within a Memory Module slot are specified below as PA[27:0]. PA[30:28] are varied for probing different Memory Module slots.

Perform the two steps below for PA[30:28] = 000, 001, 010, 011. This covers all three Memory Module pair slots.

11.2.1.1 Detection of Memory Module Presence

The first step is to check whether a Memory Module pair is present or not:

1. Perform a write to the memory block beginning at 0x0000 0000. Read back from this location.
   - If incorrect data is returned and / or an ECC error is generated, then there is no Memory Module pair at this location. Skip to the next Memory Module pair.

11.2.1.2 Determination of Memory Module Size

The next step(s) determine the base size of the Memory Module pair, if one is present:

2. Perform a write to 0x200 0000, then read from 0x000 0000. If the read does not return the data that was originally written into 0x000 0000, then this is a 16 Mbyte Memory Module.
   - A 16 Mbyte Memory Module has 25 bits of valid address, so the write to 0x200 0000 wrapped around and overwrote the contents of 0x000 0000.

3. If the correct data is returned, perform a write to 0x400 0000, then read from 0x000 0000. If the read does not return the data that was originally written into 0x000 0000, then this is a 32 Mbyte Memory Module.
   - A 32 Mbyte Memory Module has 26 bits of valid address, so the write to 0x400 0000 wrapped around and overwrote the contents of 0x000 0000.

4. If the correct data is returned, perform a write to 0x800 0000, then read from 0x000 0000. If the read does not return the data that was originally written into 0x000 0000, then this is a 64 Mbyte Memory Module.
   - A 64 Mbyte Memory Module has 27 bits of valid address, so the write to 0x800 0000 wrapped around and overwrote the contents of 0x000 0000.

5. If the correct data is returned, then this is a 128 MB Memory Module.
   - To double check, read from 0x200 0000 and 0x800 0000. All reads should return the correct data.

11.2.1.3 Completion of Probing

Write RefInterval and MEMMODPresent with the appropriate values after the probing is finished. After the probing step is performed, the actual physical memory space available in the machine is known. The boot processor can then initialize data and ECC in the entire memory space by using block writes. After this step is performed, the memory system is ready for operation.

11.3 Diagnostic

This section describes the diagnostic firmware and software tools available for troubleshooting the UltraSPARC-1 based computer. The section explains how the tools are related and when to use them. The main topics are:

- Factory-defined boot mode
- After power is switched on
- Diagnostic tools and when to use them
- Power-On Self-Test
- FORTH-based PROM diagnostics
- FORTH monitor
- SunVTS^{Tm} Diagnostic Executive.

The text in this chapter is written at the "system level" because a keyboard and some type of monitor/printer are required to view the results of the tests. The specifics of the procedures that follow must be adjusted according to the particular situation in which the USP-1 system is used.

Normally, a terminal is connected to the USP-1 computer serial port during diagnostic testing. If this is not the case with the configuration being tested, then read the documentation that is provided with the alternative equipment and adjust the following procedures accordingly.

A summary of reference materials that describe the USP-1 board is provided at the end of this chapter.

11.3.1 Factory-Defined Boot Mode

The flowcharts in Figure 12-1 and Figure 12-2 outline the roles played by various diagnostics during a *factory-defined boot* operation under the control of the OpenBoot PROM (OBP) firmware.

The following sections describe the relationship between the various diagnostic tools, and the role each tool plays during the USP-1 factory-defined boot sequence. The descriptions assume you are using a graphics monitor to view test results.

Figure 12-1 shows the Power-On Self-Test (POST) phase and Figure 12-2 shows the OBP phase. These figures graphically depict the flow of OBP processing control, after power is switched on. Each figure depicts the possible paths for processing control, and the switch settings for the factory-defined boot sequence. By examining the two flowcharts you can see where in the processing sequence other diagnostic tests are available or are encountered

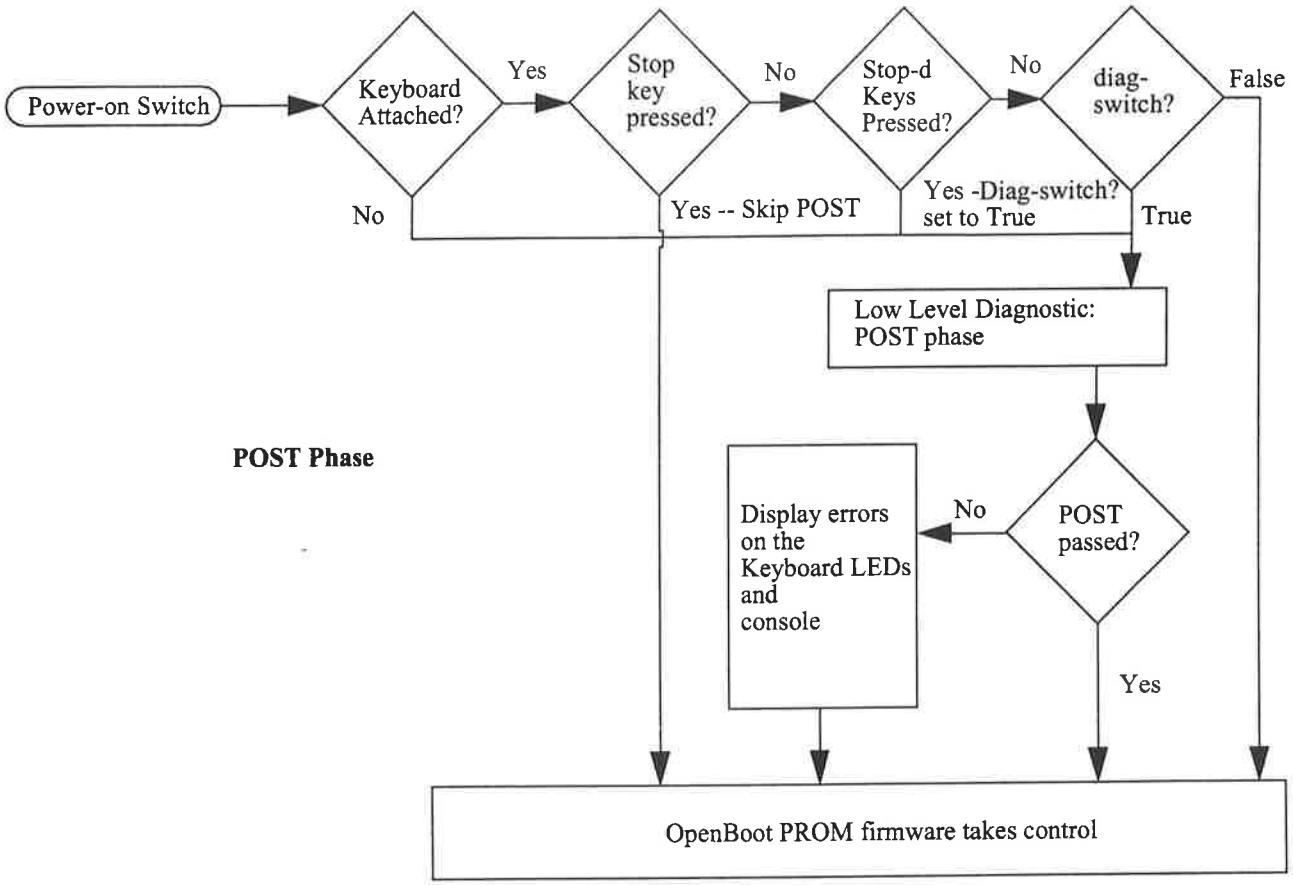


Figure 11-1. **Factory-Defined Boot Sequence-POST Phase Settings and Tests**

11.3.2 After Power Is Switched On

When you turn on the system power, the low-level POST phase is initiated if any of the following circumstances apply:

- `diag-switch?` NVRAM parameter is set to true.
- Stop-d keys are held down when you turn on the power.
- Keyboard is disconnected, and `diag-switch?` is set to false.

The low-level POST code, which is stored in the boot PROM, is designed to test the most basic functions of the system hardware. The status of the POST is conveyed by four LEDs on the Sun Type-4, Type-5, and Compact I keyboards. The Caps Lock LED blinks to indicate that the tests are in progress. If a failure is detected during low-level POST, one of the other three LEDs will light to indicate the nature of the failure (refer to Table 11-4: Interpreting the Keyboard Diagnostic LEDs).

Note — You can skip the POST phase by turning on the system while holding down the Stop key.

At the successful completion of the low-level POST phase, the OpenBoot PROM firmware takes control and performs the following initialization sequence:

- System Initialization

- Probing of the memory and then the CPU.
- Evaluation of the Script (if `use-nvramrc?` is set to TRUE).
- Probing of the SBus devices and interpreting their drivers.
- Installing the console.

After initialization, a system banner appears on the screen, and the high-level testing begins. When the high-level tests are finished, the system checks parameters stored in the NVRAM to determine the next step. Depending on the following parameter settings, the system will:

- Boot the operating system from a specified location, if `auto-boot?` is set to TRUE.
- Suppress the boot sequence and enter the FORTH Monitor (ok prompt), if `auto-boot?` is set to FALSE.
- Continually cycle through the OpenBoot PROM sequence, if `mfg-switch?` is set to TRUE.

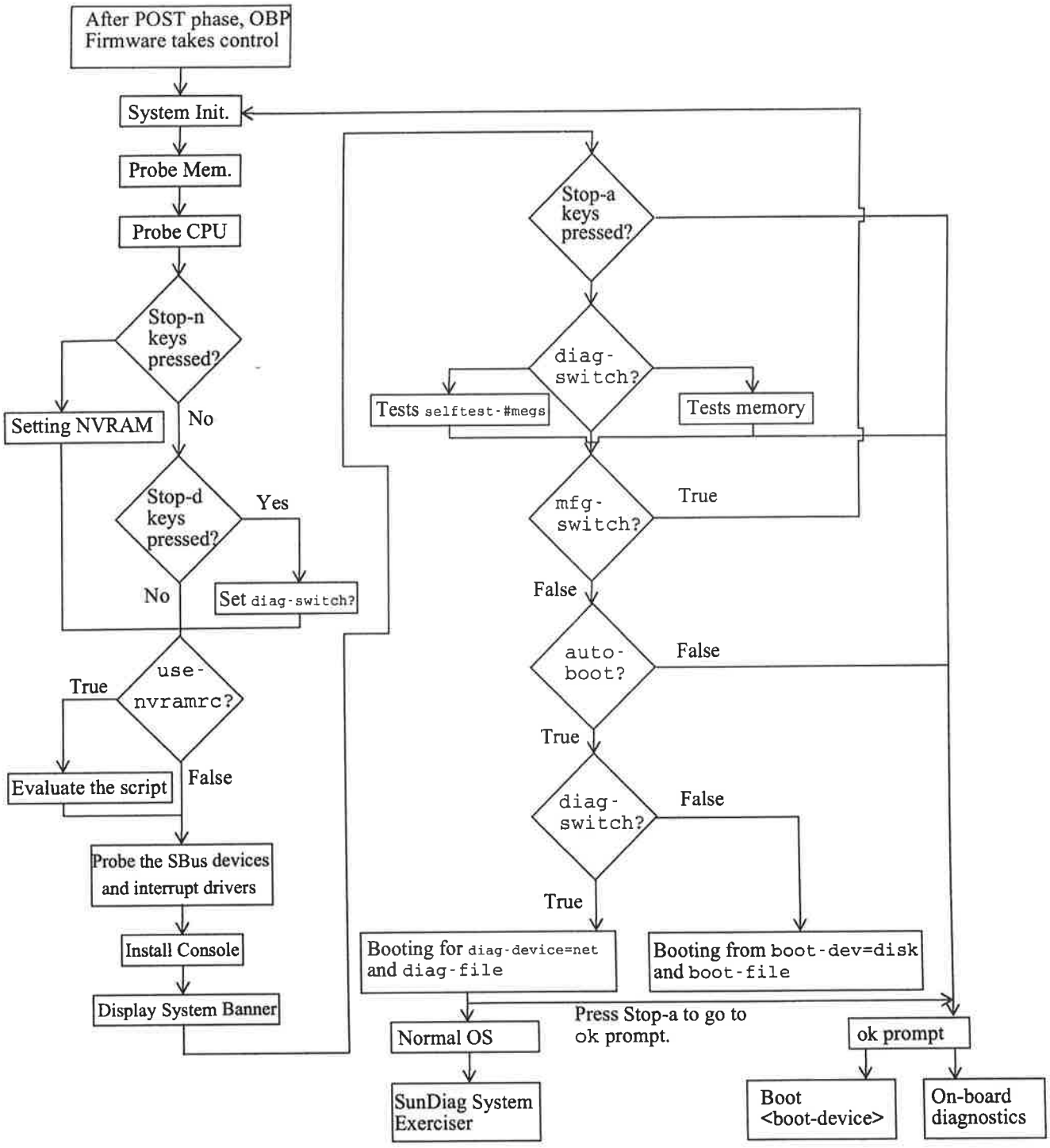


Figure 11-2. **Factory-Defined Boot Sequence: OpenBoot PROM Phase settings and Tests**

Note — If you are in the Sunmon compatibility mode (prompt is >), type 'n' to return to the OBP monitor (prompt is ok)

Table 11-1 contains a list of NVRAM parameters and explains their effects on the power-up sequence.

Note — During the high-level OBP execution, you can abort the OBP sequence and access the FORTH Monitor by pressing the Stop and "a" keys simultaneously.

Table 11-1. **NVRAM Parameters Used During POST and Boot Sequence**

NVRAM Parameter	Description

`selftest - #megs`
Default = 1
	This parameter determines how many MBytes of memory to test during high-level OBP testing if `diag-switch?` is concurrently set to false. The minimum is zero; the maximum is the amount actually installed in the system. The default is a 1-MByte test.

`diag-switch?` Default = false	When set to true, this parameter forces the system to test all available memory. It also enables diagnostic message output to Serial Port A. If a properly configured terminal or "tip window" is connected, diagnostic progress can be monitored through this port. When `auto-boot?` is set to TRUE and `diag-switch?` is set to FALSE, `diag-switch?` forces the system to boot from the device and file specified in boot-dev and boot-file.
`auto-boot?` Default = true	If `auto-boot?` is set to TRUE and `diag-switch?` is set to TRUE, the system boots the operating system from the device and file specified in the `diag-device` and `diag-file` NVRAM parameter fields. When set to FALSE, this will suppress the boot sequence. The system halts with the `ok` prompt.

At the FORTH Monitor prompt, you can direct the system to boot the operating system from a location that you specify, or you can execute a variety of additional FORTH-based tests.

If the `auto-boot?` parameter is set to true (the default), the system boots a stand-alone program. To determine from which program and device to boot, the system checks the `diag-switch?` NVRAM parameter. Table 11-2 summarizes the effect of the `auto-boot?` and `diag-switch?` parameters

Table 11-2. Summary of Autoboot and Diagnostic Switch Parameter Settings

auto-boot?	diag-switch?	Result
FALSE	FALSE or TRUE	> or `ok` prompt
TRUE	FALSE	Boots the operating system from device alias "disk" or ".net" for SPARCstation 5 system.
TRUE	TRUE	Boot operating system from device alias "net"

Note — The boot parameters represented here are default settings. The defaults may be changed by following the procedures listed in the *OpenBoot Command* Summary.

Once the operating system is running, you can invoke the SunDiag System Exerciser if further diagnostic testing is warranted.

Another stand-alone diagnostic program you can run is the SunDiagnostic Executive.

To boot user-specified programs, such as the SunDiagnostic Executive, you must be at the > prompt or `ok>` prompt.

11.3.3 Diagnostic Tools and When to Use Them

Table 12-3 provides a summary of the available USP-1 board diagnostic tools and describes when to use each tool.

Table 11-3. USP-1 Board Diagnostic Tools

Diagnostic Tool	When or Why to Use the Tool
Power-On Self-Test (POST)	Executes automatically at power-on when Stop-d keys are pressed or when the `diag-switch?` parameter is set to true. The POST code resides in the boot PROM and is driven by the POR signal from the power supply. POST tells you if there is a problem with the main logic board, the NVRAM, or the Memory Modules
FORTH Diagnostics	Tests functions such as the Ethernet and SCSI interfaces, system memory, and the diskette drive controller. You must be at the `ok>` prompt (the FORTH Monitor) to run the FORTH Diagnostics. The FORTH Diagnostics reside in the boot PROM.
FORTH Monitor	Allows input to the system at the boot PROM level. Supports functions such as changing NVRAM parameters, resetting the system, running diagnostic tests, displaying system information, and redirecting input and output. See the *OpenBoot Command Reference* for more information.
SunVTS	Allows the user to determine real-time use of system resources and peripheral equipment.

11.3.4 Power-On Self-Test

The Power-On Self-Test (POST) runs when you turn on the system unit power switch and any of the following conditions apply:

1. `diag-switch?` NVRAM parameter is set to TRUE.
2. Stop-d keys are held down when you turn on the power.
3. Keyboard is disconnected, and `diag-switch?` is set to FALSE.

The POST comprises a sequence of tests designed to evaluate the major hardware components of the main logic board in the short time before the OpenBoot PROM firmware takes control. The POST does not perform extensive testing on any component of the main logic board. Only major failures can be detected by the POST.

Four different LEDs on the keyboard are used to indicate the progress and results of the POST. These LEDs are on the Caps Lock, Compose, Scroll Lock, and Num Lock keys. To indicate the beginning of the POSTS, the four LEDs briefly light all at once. The monitor screen remains blank, and the Caps Lock LED blinks for the duration of the POST.

If the system fails any POST, one of the LEDs will light to indicate the nature of the problem. The LED may be lit continuously, or for just a few seconds. Table 12-4 provides the meaning of each diagnostic LED.

Note — The keyboard LEDs may illuminate in a different sequence and for different reasons depending on what type of keyboard is connected to the system in which the USP-1 board is installed. The information in Table 11-4 has been derived from a SPARCstation 5 workstation using a Sun Type-5 keyboard.

Table 11-4. Interpreting the Keyboard Diagnostic LEDs

Diagnostic LED	Failed Part
Num Lock LED is lit	Main logic board
Scroll Lock LED is lit	NVRAM
Compose LED is lit	DSWM

Note — The Caps Lock LED is not used as a failure indicator; it flashes on and off to indicate that the POSTs are running.

11.3.5 FORTH Monitor

The FORTH Monitor is a basic diagnostic utility and system interface. If there is any problem with your operating system, the FORTH Monitor automatically starts, as indicated by the appearance of the `ok>` prompt (the FORTH Monitor also starts if `auto-boot?` is set to FALSE).

You can also choose to access the FORTH Monitor by halting the system. For additional information about tests you can run from the FORTH Monitor, see *OpenBoot Command Reference.*

11.3.5.1 FORTH-Based PROM Diagnostics

Table 12-5 lists specific FORTH-based on-board diagnostic tests for the USP-1.

Table 11-5. Selected FORTH Diagnostic Tests

Type of Test	Description	Preparation	When to Use
`test screen`	Tests the system video graphics hardware and monitor.	The `diag-switch?` NVRAM parameter must be set to TRUE	See description.
`test floppy`	Tests the floppy drive response to commands.	Insert a formatted diskette into the drive.	See description.
`test scsi`	Tests the SCSI interface logic on the system board.	The `diag-switch?` NVRAM parameter must be set to TRUE.	See description.
`test net-aui`	Performs an internal and an external loopback test on the AUI (Thick) Ethernet interface.	A cable must be connected to the system AUI Ethernet port and to an Ethernet tap or the test will fail the external loopback phase.	See description.
`test net-tpe`	Performs an internal and an external loopback test on the twisted-pair Ethernet (TPE) interface.	A cable must be connected to the system AUI Ethernet port and to an Ethernet tap or the test will fail the external loopback phase.	See description.
`test net`	Performs an internal and an external loopback test on the auto-selected system Ethernet interface.	A cable must be attached to the system and to an Ethernet tap or hub or the external loopback test will fail.	See description.

`test disk`
`test disk0`
`test disk1`
`test disk2`
`test disk3`
	Tests internal or external SCSI disks that have a self-diagnostic program contained in the drive control (disk0 = SCSI address 0, disk1 SCSI address 1, disk2 = SCSI address 2, disk and disk3 = SCSI address 3).	The drive must be spinning before this test is executed or the test will fail.
		
		Enter a `boot` *<disk alias>* command to cause the drive to spin up.
			See description.

`test cdrom`	Performs a self-test diagnostic on the CD-ROM drive.	The CD-ROM must be set to SCSI target 6 and have a CD will the test will fail.	See description.

`test tape`
`test tape0`
`test tape1`
	Tests the SCSI tape drive by executing the drive self-test program. tape and tape 0 are located on the first tape drive. Tape 1 is located on the second tape drive.	Connect the tape drive to the system and then turn on the power.	See description.

Table 11-5. Selected FORTH Diagnostic Tests

Type of Test	Description	Preparation	When to Use
`test ttya` `test ttyb`	Outputs an alphanumeric test pattern on the system serial ports (ttya = serial port A) (ttyb = serial port B).	Attach a terminal to the serial port to observe the output.	Tests serial ports
`test keyboard`	This test executes the keyboard self-test. The four LEDs on the keyboard flash on and the message Keyboard Present is displayed.	Keyboard must be connected.	See description.
`test-memory`	Test all of the system main memory if the `diag-switch?` is true. If `diag-switch?` is set to false, it tests the memory according to the number specified in `self-test-#megs`.	None.	See description.
`test-all`	Test all devices in the system (such as SBus cards) that have a built-in test program. Hard disks, tapes, and CD-ROMs are not tested.	Set the `diag-switch?` NVRAM parameter to true.	When a device driven by an SBus card is not functioning properly.
`watch-clock`	Displays seconds from the system's Time-of-Day chip.	None.	See description.
`watch-net`	Monitors broadcast Ethernet packets on the Ethernet cable(s) connected to the system.	Connect the system to the network via the desired Ethernet port.	See description.
`watch-aui`	Monitors broadcast Ethernet packets (10Base5 -- Thicknet) on the Ethernet cable(s) connected to the system.	Connect the system to the network via the desired Ethernet port.	See description.
`watch-tpe`	Monitors broadcast Ethernet packets (10BaseT -- Twisted - Pair Ethernet) on the Ethernet cable(s) connected to the system.	Connect the system to the network via the desired Ethernet port.	See description.
`watch-net-all`	Monitors broadcast Ethernet packets on all Ethernet interfaces installed in the system, one at a time.	Connect the system to the network via the desired Ethernet port.	When an SBus card network controller card is installed.

Table 11-5. Selected FORTH Diagnostic Tests

Type of Test	Description	Preparation	When to Use
`probe-scsi`	Returns the SCSI devices (internal and external) and their SCSI targets connected to the built-in SCSI port.	Connect external SCSI devices to the system and turn on their power.	To determine if a SCSI peripheral is talking to the system. To determine the SCSI targets (addresses) of a SCSI device. To determine if more than one SCSI peripheral is assigned the same SCSI address To determine if the built-in SCSI controller is defective.
`probe-scsi-all`	Returns to the display the SCSI devices and their SCSI targets connected to all SCSI ports (both the built-in SCSI port and any additional SCSI host adapter cards).	Connect external SCSI devices to the system and turn on their power.	See `probe-scsi`. To determine if a SCSI host adapter controller is defective.
`power-off`	Powers off the system.	You must have a Sun Type-5 keyboard in order to use this command.	To power off the system with a Sun Type-5 keyboard.

11.3.6 SunVTS

Use SunVTS programs to determine real-time use of system resources and peripheral equipment such as Desktop Storage Modules and External Storage Modules. SunVTS programs can be written to verify that the system is functioning properly. For information about how to use SunVTS, see the *SunVTS 1.0 Test Reference Manual and SunVTS 1.0 User's Guide.*

If SunVTS passes, the system is operating properly. If it fails, the error messages should indicate the part of the system that has failed. If the error messages are not descriptive enough, you may need to run POST.

UPA address parity can be checked in the U2S through the use of the APCKEN and APERR bits. Software will write the APCKEN bit to '0', disabling parity checking on the address. Then, the IAP bit is set in the System Controller, and a transaction is run to the U2S. It should report the error through the APERR bit, but the transaction will complete as though the address had no parity error.

Testing the address parity checking logic in the System Controller is more complex. Invalid addresses delivered to the System Controller result in a FATAL error being generated, which results in a reset of the system. Diagnostics will therefore have to set up a 'mailbox' in NVRAM, perhaps, which indicates that the error reset condition is desirable. Then, using the IAP bit in the U2S, a transaction can be run. This can consist of any U2S mastered transaction, such as a DVMA operation, or a Flush Synchronization operation. With the IAP bit set, a FATAL condition is generated and will result in a system wide reset.

11.4 10Base-T Twisted Pair Ethernet Link Test

11.4.1 Scope

Read this chapter if you are connecting your USP-1 system to a 10Base-T twisted-pair Ethernet (TPE) network. This chapter contains important information for getting your system to communicate correctly over a TPE network. If you have no experience with TPE networks, ask your system or network administrator to perform the procedures in this chapter. The USP-1 does not support signal quality error (SQE) detection.

11.4.2 Overview

- The twisted-pair Ethernet link integrity test is a function defined by the IEEE 802.3 10Base-T specification.
- For a network workstation (host) to communicate with a network hub, the link test state (enabled or disabled) must be the same on the host and hub.
- If either the host or hub does not share the link test enabled / disabled state of the other, then the host cannot communicate effectively with the hub, and the hub cannot communicate effectively with the host.

Figure 12-3 gives an example of a star configuration local area network (LAN) and demonstrates the relationship of hosts to a hub.

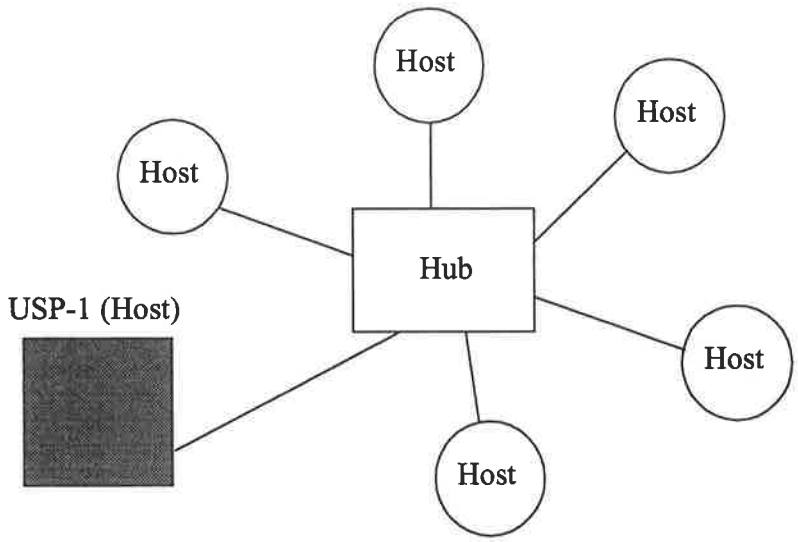


Figure 11-3. **Hosts and Hub in a Local Area Network**

Figure 12-4 shows the importance of ensuring that the host and hub link test settings match in a 10Base-T network.

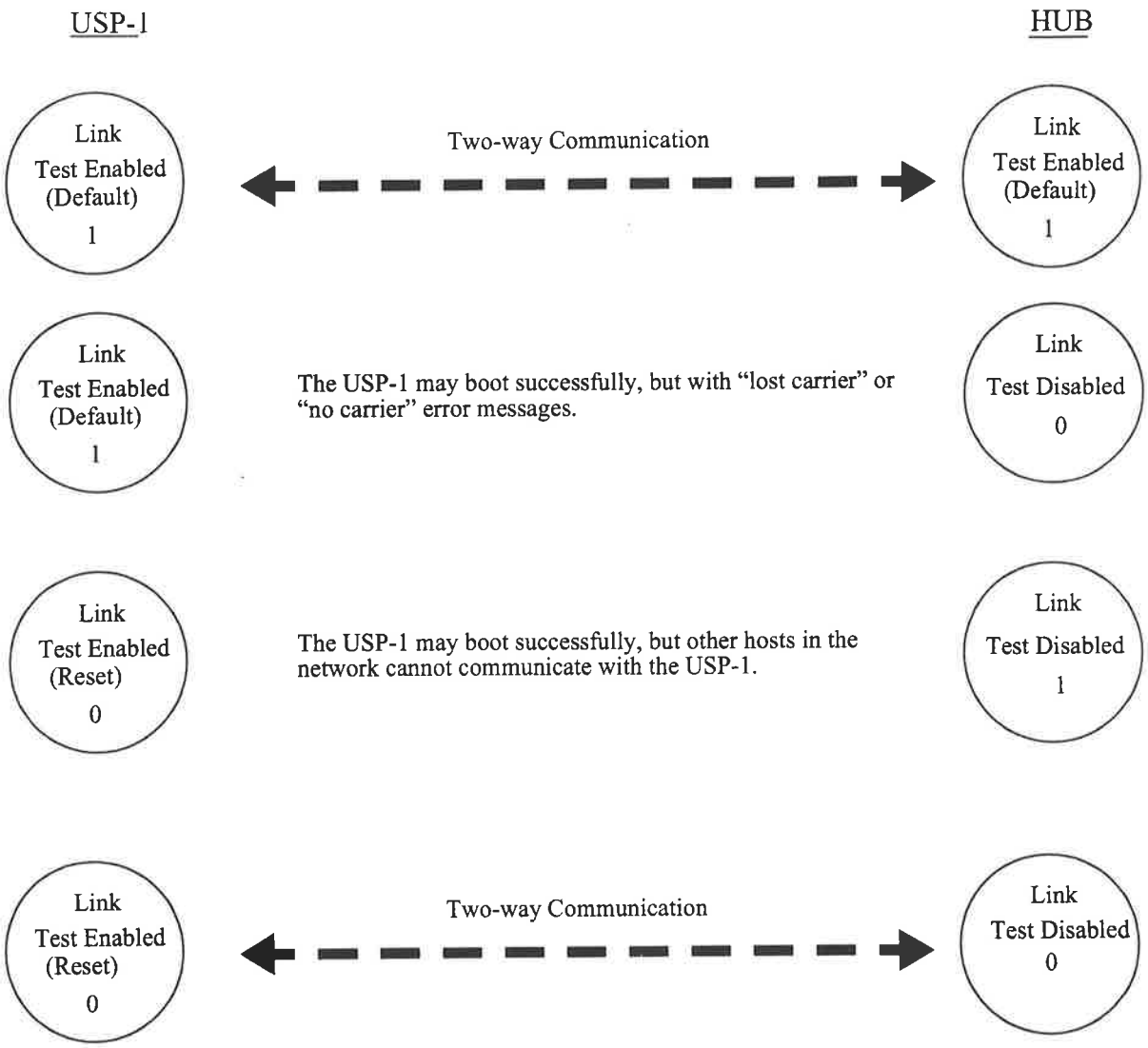


Figure 11-4. **Ensuring Host-Hub Communication in a 10Base-T Network**

11.4.3 Technical Discussions

The twisted-pair Ethernet link integrity test determines the state of the twisted pair cable link between the host and the hub in a network. Both the host and hub regularly transmit a link test pulse. When either the host or hub has not received a link test pulse within a certain amount of time (50-150 ms), it makes the transition from the link-pass state to the link-fail state and remains in the link-fail state until it once again receives regular link test pulses.

The link integrity test is specific to twisted-pair Ethernet and is not applicable to the other physical layer implementations of IEEE 802.3 such as 10BASE5 ("thicknet") or 10Base2 ("thinnet").

The link test function at the host or hub is either enabled (link test enabled or 1) or disabled (link test disabled or 0). The IEEE 802.3 10BASE-T specification requires that the link test be enabled at both the host and the hub.

Although link test disabled does not conform to the specification, it is often encountered real-world 10Base-T network installations. Some hubs from various vendors can exhibit any of the following:

- Link test is "hardwired" enabled-link test is always enabled.
- Link test is "hardwired" disabled-link test is always disabled.
- Link test is configurable-the network administrator may enable or disable link test.

11.4.4 Troubleshooting

If you have connected an USP-1 host to a hub using twisted-pair Ethernet cable and observe either "no carrier" messages or fail to communicate effectively with another host in the same network, look first at the hub. If it supports configurable link test, then make sure "link test enabled" is configured. This is usually done by setting a hardware switch.

If the hub does not support configurable link test, then refer to the hub manufacturer's documentation. Check to see if your hub is hard-wired for link test disabled. If it is, you must follow the "Checking or Disabling the Link Test" procedure elsewhere in this chapter to disable the link test at your USP-1 host.

11.4.5 Enabling the Link Test

1. If you do not see the ok prompt, press the Stop (Ll)-a keys.

2. At the `ok` prompt, type:

```
ok printenv tpe-link-test?

tpe-link-test?            false                    false

ok
```

The above screen shows the current link test state (FALSE, or disabled), followed by the default state (TRUE, or enabled).

3. To enable the host's link test function, type the following commands:

```
ok setenv tpe-link-test? true

tpe-link-test?          true

ok reset-all
```

4. Boot the host and verify that the transceiver cable problem messages do not appear. Type either `boot net` or `boot disk` and press Return.

11.4.6 Moves and Changes

Unless the new network relationship between the host and the hub is functional (that is, 1-1 link test enabled-link test enabled or 0-0 link test disabled-link test disabled), there will be no full, regular two-way communication between the host and the hub.

11.4.7 Checking or Disabling the Link Test

To check the link test state of an USP-1 host:

1. If you do not see the ok prompt, press the Stop (L1)-a keys.

2. At the ok prompt, type:

```
ok printenv tpe-link-test?

tpe-link-test? true true ok
```

The above illustrates the current link test state (TRUE, or enabled), followed by the default state (TRUE, or enabled).

To disable the host's link test function:

3. Type the following commands:

```
ok setenv tpe-link-test? false

tpe-link-test?          false

ok reset-all
```

4. Boot the host and verify that the transceiver cable problem messages do not appear. Type either `boot net` or `boot disk` and press Return.

11.5 Reference Materials

The following reference materials from Sun Microsystems provide a complete definition of the USP-1 on-board diagnostics, and current diagnostic tools:

- *SunVTS 1.0 User's Guide* (Sun Part No. 801-7271)
- *SunVTS 1.0 Test Reference Manual* (Sun Part No. 801-1448)
- *SunVTS 1.0 Quick Reference Card* (Sun Part No. 801-3672)
- *Open Boot 3.x Command Reference* (Sun Part No. 802-3242)
- *OpenBoot 3.0 Command Summary* (Sun Part No. 802-xxxx)
- *Writing FCode 3.x Programs* (Sun Part No. 802-xxxx)
- *SBus Developer's Kit II+* (Sun Part No. 605-1307)

12

JTAG

12.1 Overview

JTAG is an acronym for Joint Test Action Group. This group defined a method of accessing the test features of digital systems. The method is specified in the IEEE 1149.1-1990 Standard Test Access Port document.

In general, JTAG uses a serial bit stream to control a state machine which can select, read, and write shift registers of various lengths. These shift registers can in turn be used to control different test modes and test features of the system and its components.

The test modes of the system includes internal scan and boundary scan of the ASICs, and partial interconnect test of the system board. The reason that the interconnect test of the system is only partial, is that not all of the components in the system have a JTAG port. Since this is the case, JTAG boundary scan and the normal manufacturing in-circuit test are used to completely test the system board interconnects.

In addition, some test features will include a built in self test (BIST) of some memories in the ASICs and a scan dump of internal scan chains of the ASICs.

The group of signals that control the serial bit stream is known as the JTAG port. The JTAG port for SBus Reference Platform systems will utilize five signals. These signals are: serial test data input (TDI), serial test data output (TDO), test mode select (TMS), test clock (TCK), and asynchronous reset (TRST_).

Table 12-1. **JTAG Port Signals**

Signal	Function
TDI	Serial bit stream for JTAG input data
TDO	Serial bit stream for JTAG output data
TMS	Serial bit stream for controlling JTAG state machine
TCK	JTAG Clock
TRST_	Asynchronous JTAG state machine reset (active low)

12.2 Goals

The goals of using JTAG and scan methodology on USP-1 are as follows:

- Provide 100% opens and shorts testing on the system board, combination of in-circuit test and JTAG.
- Enable in-circuit test to use boundary scan to test BGA packages.
- Exceed 96% testable fault coverage of new ASICs.
- Enable ScanTool to test the system board.
- Enable ScanTool to run ATPG test on new ASICs.

12.2.1 System JTAG Architecture

There is a single major scan chain for the JTAG components on the system board. The single major scan chain on the system board will enable manufacturing to use their in-circuit test machines to activate the JTAG port without any modules plugged in.

The independent scan chains for the modules allows ScanTool to activate the JTAG port of any scan chain in the system. ScanTool will be able to run tests on the major scan chain and also the scan chain for each module.

12.2.2 USP - 1

The USP -1 has one scan ring. The scan ring contains all the JTAG compatible components on the system board.

12.3 ScanTool Specifics

ScanTool (third party scantool) can execute different tests on the system hardware through the JTAG port.

12.3.1 Operating Frequencies

In-circuit tests will use JTAG boundary scan at 5 MHz. All JTAG compatible components will run boundary scan at 5 MHz.

12.3.2 I/O Voltage Levels

The following are the voltage levels of signals in the system board scan chain (the 3v TTL outputs can drive 5v TTL inputs, but 5v TTL outputs cannot drive 3v TTL inputs, unless they are +5V tolerant).

Table 12-2. **I/O voltage levels**

Chips	TDI	TDO	TMS	TCK	TRST_
RIC	5	3.3	5	5	5
UltraSPARC-1	3.3	3.3	3.3	3.3	3.3
SRAMS	3.3	3.3	3.3	3.3	3.3
UDB	3.3	3.3	3.3	3.3	3.3
USC	5	3.3	5	5	5
U2S	5	3.3	5	5	5
APC	5	5	5	5	5
MACIO	5	5	5	5	5
SLAVIO	5	5	5	5	5

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